# Reliability Comparison of 28 V – 50 V GaN-on-SiC S-Band and X-Band Technologies

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***Abstract*— This paper discusses the reliability performance of Wolfspeed GaN/AlGaN high electron mobility transistor (HEMT) MMIC released process technologies, fabricated on 100 mm high purity semi-insulating (HPSI) 4H-SiC substrates. The intrinsic reliability performance of the 28 V and 40 V technologies, with 400 nm and 250 nm gate length, has been characterized with DC accelerated life test (DC-ALT), for which ohmic contact inter-diffusion is the wear-out mechanism, and is accelerated by temperature and current. The intrinsic reliability performance of the 50 V technologies, with 400 nm gate length, have been characterized with RF-ALT, for which source-connected second field plate void coalescence is the wear-out mechanism, and is accelerated by temperature. In spite of the differences in the accelerated test methodologies and wear-out mechanisms, all of the Wolfspeed GaN-on-SiC technologies demonstrate high and similar predicted lifetimes at their respective maximum recommended operating conditions. The reliability performance is supported with successful technology qualifications with zero failures, and volume manufacturing with a demonstrated low field failure rate.**

***Keywords— GaN; SiC; HEMT; DC-ALT; RF-ALT; intrinsic reliability; wear-out***

## I. Introduction

Wolfspeed currently manufactures and sells a complete line of commercial GaN discrete transistors for both general purpose (military, civil, industrial, and scientific) and wireless (4G/5G, LTE, etc.) applications. The general purpose discrete parts currently support a number of military systems including communications, jammers, radar, and a variety of other industrial applications. Wolfspeed also develops and produces high-power GaN MMIC products to support a variety of commercial and defense applications. These have been successfully fielded in a variety of harsh application environments.

The 0.4 µm gate length process technology (V3) is offered in 28 V and 50 V variants (G28V3 and G50V3) optimized for their respective applications – typically S-band or broad band frequencies. The G50V3 process technology has several variants with optimization for linearity and gain. The 0.25 µm gate length process technology (V4) is offered in 28 V and 40 V variants (G28V4 and G40V4), optimized for their respective applications – typically in the X and Ku bands. All of these processes offer MIM capacitors (180 pF/mm2), NiCr thin film resistors (12 Ω/square), and low-resistance source vias that are small enough to embed inside the transistor technology. All of these processes are fully qualified and released for volume manufacturing.

The G28V3 intrinsic reliability performance and technology qualification on 100 mm SiC wafers were summarized by Gajewski et al., in 2011 [1]. Wolfspeed's G28V3 and G28V4 Title III production-capacity program and Manufacturing Readiness Level Eight (MRL8) achievement was summarized by Fury et al., in 2013 [2]. The Wolfspeed V4 technology, performance and target applications were summarized by Wood et al., in 2013 [3]. The reliability performance, and the characterization and elimination of an early life failure (ELF) mechanism that only occurs under accelerated life test (ALT) conditions, of the G40V4 process, was summarized by Gajewski et al., in 2014 [4].

## II. Experimental

### A. Device fabrication

All of the devices discussed in this paper consist of discrete high electron mobility transistor (HEMT) devices with 3.6 mm total gate periphery. The GaN-on-SiC HEMT wafers were fabricated and processed on 100 mm high purity semi-insulating (HPSI) 4H-SiC substrates, and the devices were assembled, at Wolfspeed, in Research Triangle Park, NC, USA. The devices were assembled using the production process for Cree's released product CGH40010F, which features a 1:1:1 CuMoCu cavity-style package with AuSn eutectic die attach, and gold wire bonds.

### B. Determining junction temperature

For normal operation, qualification, and reliability tests, the channel temperature is estimated as the maximum junction temperature in the channel just under the gate corner on the drain side. Infrared (IR) microscopy and finite element analysis (FEA) are employed to produce accurate channel to case temperature differentials, from which a θjc (peak junction to case thermal resistance) is calculated. An iterative process is employed, in which an IR image is taken for a given power dissipation and base plate temperature. The FEA is the spatially averaged and compared with the IR image. The thermal resistance is a modeled parameter that is adjusted iteratively until agreement is achieved between the IR and FEA. The resulting thermal resistance is then used to estimate the maximum junction temperature for a given power dissipation and case temperature, as described in [5].

### C. Reliability testing

Intrinsic reliability tests are defined as die-level tests that are meant to stress devices under highly accelerated conditions. The goal is to determine device lifetime statistics that can be modeled

to predict the device lifetime at maximum recommended operating conditions.

Extrinsic reliability qualification tests characterize the die, package, and/or die-package interaction reliability under maximum recommended normal operating conditions. The tests are meant to exercise any weaknesses or defects that may lead to early life field failures. The goal is to demonstrate product reliability with zero failures.

*1) DC-ALT / high temperarture operating life (HTOL)*

DC-ALT/HTOL is performed under DC drive conditions at the nominal drain operating voltage (28 V, 40 V, or 50 V) and high dissipated power that is typical for many target applications (6 W/mm). The current is held constant throughout the test by individual gate control circuits for each device. Since all of the technologies were stressed at 6 W/mm, the higher voltage technologies encounter correspondingly lower stress current. The base plate temperature of the thermal platform is set and actively controlled to ensure that the average device peak junction temperature target is achieved. The average peak junction temperature is estimated using thermocouples attached to the flanges of a sampling of devices, and the thermal model as described above.

- DC-ALT is an intrinsic test. It is conducted by stress-measure-stress cycles, where devices are stressed for a period of time, and then removed from the test system for down-point test of a comprehensive suite of DC and RF device parameters at room temperature, and then the stress is continued until failure or enough degradation has been achieved that the lifetime can be determined by extrapolation.
- DC-HTOL is an extrinsic test. It is run for 1000 hours without interruption, followed by final test of a comprehensive suite of DC and RF device parameters at room temperature.

*2) RF- ALT / high temperarture operating life (HTOL)*

RF-ALT/HTOL is performed under RF drive conditions at the nominal drain operating voltage (28 V, 40 V, or 50 V) and high RF compression level that is typical for many target applications. The tests were conducted using a commercial reliability test system manufactured by the Accel-RF Instruments Corporation. The devices are biased to 200 mA quiescent current and constant input power of 29 dBm, which results in an output power of approximately 43 dBm and RF gain compression of approximately 3 – 5 dB. Each device fixture has its own individual heater block that actively controls its temperature in real time throughout the test in order to maintain a constant junction temperature, as computed by the block temperature, dissipated power, and thermal model.

- RF-ALT is an intrinsic test. It is run until device parametric failure or catastrophic failure or conclusion of the test. The devices are not taken off the system for any ex-situ down points.
- RF-HTOL is an extrinsic test. It is run for 1000 hours without interruption, followed by final test of a comprehensive suite of DC and RF device parameters at room temperature.

*3) High temperarture reverse bias (HTRB)*

HTRB testing is meant to represent continuous exposure of the die and package to the maximum recommended case temperature at worst case reverse bias pinch-off condition. The HTRB is run at 2.5 – 3 times the nominal operating drain voltage to simulate the maximum drain voltage that may be encountered in typical RF applications. The test is meant to exercise any high electric field failure modes and any die-level defects that may lead to early life field failures.

### *D. Device failure criteria*

A device failure is defined as a condition in which a stressed device has a 1 dB change in critical RF parameters (small signal gain, saturated power (Psat), or saturated power drain efficiency), 20% change in saturated drain current or on-resistance, loss of pinch-off gate control, or has consequential external physical damage attributable to an environmental test. For ALT, for any devices that did not reach a failure criterion by the conclusion of the test, their lifetimes were estimated by extrapolating the Psat degradation to 1dB decrease from its initial value, using an empirically determined functional form for the time dependence.

## III. RESULTS

### *A. DC-ALT*

For the DC-ALT, the RF saturated output power (PSAT) was the parameter that degraded the most significantly, across all of the DC and RF device parameters tested at down points. Therefore, the PSAT determines the device failure criterion and device lifetime.

*1) 28 V – 40 V technologies*

Fig. 1 shows a representative result of the PSAT degradation versus stress time for a population of G28V3 devices under DC-ALT conditions ranging from approximately (350 – 380) °C junction temperature. The result shows that PSAT degrades over time in a fairly well behaved fashion, with no abrupt or large changes. Empirically, the time dependence is observed to degrade as approximately sqrt(time), although the number of down points limits the ability to determine the functional form with a great deal of statistical confidence. The individual device lifetimes were determined by fitting the degradation to a sqrt(time) model and either interpolating or extrapolating to -1 dB. Fig. 1 shows that even after nearly 5000 hours of stress at a highly accelerated condition, most devices still did not reach the -1 dB failure criterion. Therefore, the lifetimes of many of the devices had to be determined by extrapolation of a sqrt(time) fit. The degradation rate was found to be accelerated with junction temperature. This result is typical for temperatures across the ALT temperature range tested, and is similar to results obtained for G28V4 and G40V4. These results are consistent with a common wear-out mechanism for the G28V3, G28V4, and G40V4 technologies.

The PSAT degradation results are qualitatively consistent with a wear-out mechanism that occurs gradually over time, for example, material diffusion. The results are not qualitatively consistent a wear-out mechanism that results in abrupt and large changes in the device performance, for example, as has been reported by other institutions in the literature for the piezo-electric cracking failure mechanism [6]. Previous Wolfspeed

publications have shown by physical failure analysis that the wear-out mechanism is source-side ohmic contact inter-diffusion and associated on-resistance increase, that results in the PSAT degradation; and that no evidence of piezo-electric cracking was observed after 28 V and 40 V ALT [1, 4]. The failure analysis showed that the ohmic contact inter-diffusion occurs only on the source side and not the drain side. Given that the source and drain ohmic contact materials stacks are identical, this indicates that the ohmic contact inter-diffusion is accelerated by the direction of electrical current flow.

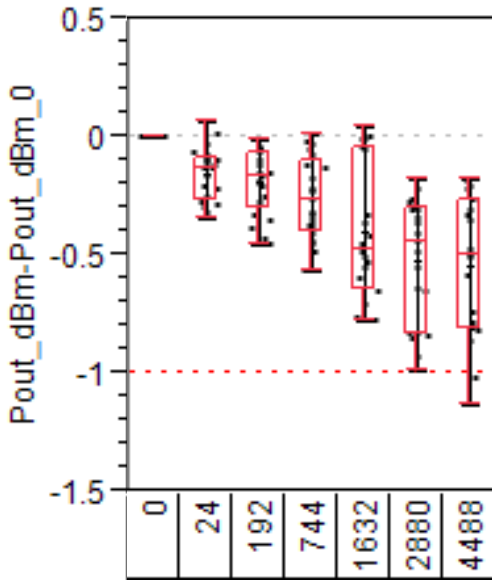


Fig. 1. Representative saturated output power degradation (dB) versus hours for G28V3 technology DC-ALT at a typical accelerated stress junction temperature. Each data point represents one device under test at its corresponding down point duration. The red line indicates the failure criterion of -1 dB.

DC-ALT data at multiple temperatures was used to construct the lifetime prediction curves for G28V3 and G28V4 shown in Fig. 2. The curves were generated by fitting the lifetime distributions at the stress temperatures, using lognormal statistics and maximum likelihood estimation to extract the time to 1% failures, with statistical confidence bounds. The results give activation energies of 1.7 eV and 1.4 eV for G28V3 and G28V4, respectively.

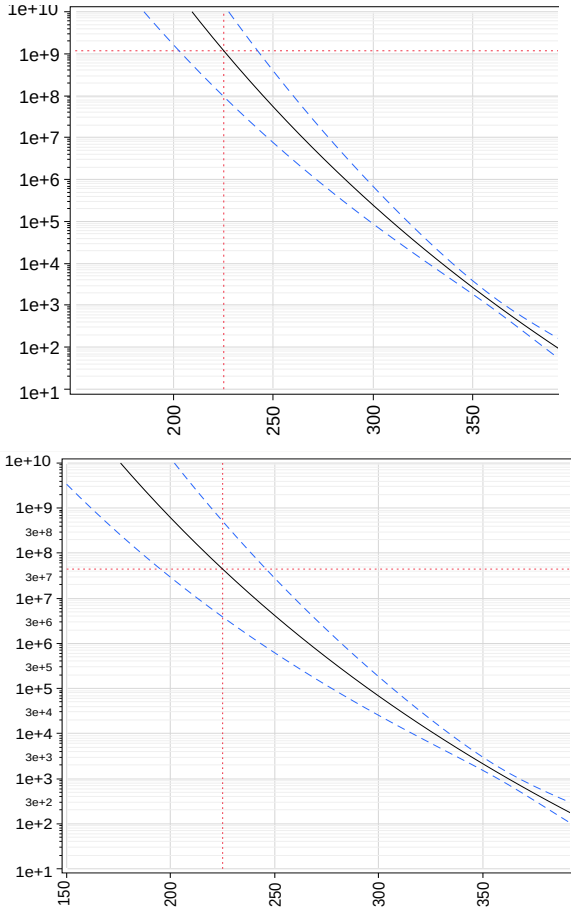


Fig. 2. DC-ALT intrinsic lifetime prediction of G28V3 (upper) and G28V4 (lower) technolgoies. Solid line shows the time (hours) to 1%-ile failures, and dashed lines show 80% 2-sided (90% 1-sided) statistical confidence bounds, versus junction temperature.

The G40V4 DC-ALT showed similar PSAT degradation trends and ohmic contact inter-diffusion. The intrinsic lifetime curve showed an activation energy of 1.2 eV and a t1% of 7E5 hours at 200 °C junction temperature [4].

The activation energies are close enough in value, within the variation has been measured over various other tests, to be confident that the activation energy and wear-out mechanism is the same for G28V3, G28V4, and G40V4.

*2) 50 V technologies*

The PSAT degradation observed for the Wolfspeed 50 V technologies is appreciably different than that of the 28 V – 40 V technologies. Fig. 2 shows the PSAT degradation for a population of devices at a highly accelerated junction temperature. The results show that PSAT degrades by approximately -0.3 dB after the first down point, but then degrades very little or imperceptibly so (within the precision of the measurement) for the remainder of the ALT. Although Fig. 2 shows that the initial degradation occurs after 36 hours, other ALT testing has shown that the 36-hour value is not critical; similar degradation trends have been seen after just a few hours of 50 V ALT. This suggests that the initial degradation is likely related to trapping or possibly a very minor burning-in of the device.

The fact that the PSAT degradation does not increase over time, even over thousands of hours at the highest junction temperature DC-ALT condition, suggests that the lower current of the 50 V ALT does not produce the same level of ohmic contact inter-diffusion that it does in the 28 V – 40 V technologies. This lack of degradation over time has been confirmed with failure analysis that found no evidence of ohmic contact inter-diffusion. This type of DC-ALT testing has been repeated many times for these technologies, and the result is consistent. Since the current in the 50 V ALT is only 44% lower than it is for 28 V ALT and 20% lower than it is for 40 V ALT, this suggests that the current dependence of the ohmic contact inter-diffusion is relatively high. Although degradation does not appear to behave as sqrt(time), such a fit was made to that data, in order to extract a set of device lifetimes in a consistent manner as was done for the other technologies. Due to the extent to which the extrapolation had to be made, the uncertainties are high, and so intrinsic lifetime extrapolations are that much higher, being an extrapolation of a set of extrapolations. Therefore, only the median values are shown in Fig. 4.

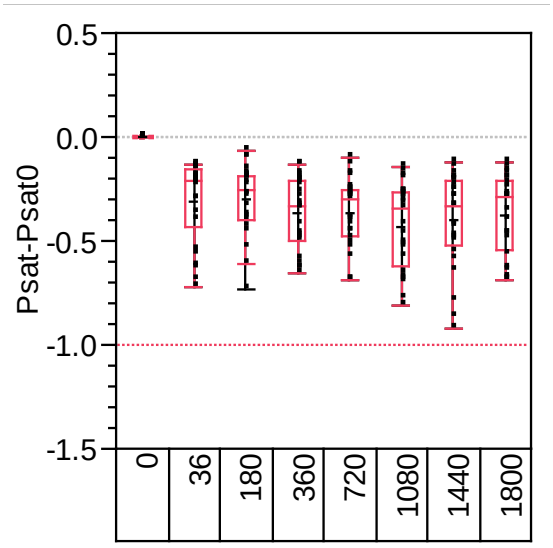


Fig. 3. Representative PSAT degradation (dB) versus hours for G50V3 technology DC-ALT at a typical accelerated stress junction temperature. Each data point represents one device under test at its corresponding down point duration. The red line indicates the failure criterion of -1 dB.

### *B. RF-ALT*

In order to confirm the intrinsic lifetime predictions of the DC-ALT, and to obtain more confidence in the predictions for the 50 V technology, RF-ALT was performed. Fig. 4 shows a representative output power response at RF-ALT conditions. The output power at RF-ALT conditions initially degrades smoothly and monotonically, and then after some period of time, catastrophic failures start occurring before the devices reach a parametric failure criterion of -1 dB. This result is typical for junction temperatures ranging from (350 – 425) °C.

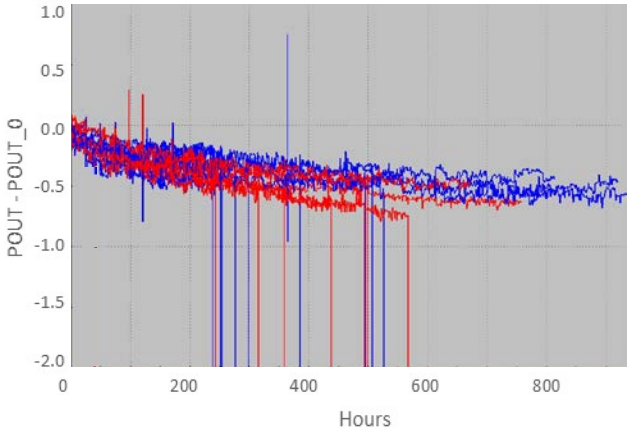


Fig. 4. Representative POUT degradation (dB) versus hours for a set of G50V3 devices under RF-ALT at a typical accelerated stress junction temperature. The red and blue curves represent sets of devices that can be considered equivalent for the purposes of this test.

An accelerated life fit to the RF-ALT data versus junction temperature, using lognormal statistics, gave an activation energy of 1.6 eV and intrinsic lifetime prediction shown in Fig. 5. The RF-ALT prediction likely has a great deal more statistical confidence, since nearly all devices reached failure, rather than in DC-ALT where most device lifetimes had to be extrapolated. The DC-ALT prediction is likely conservative due to the sqrt(time) fit to the data; in reality, the time dependence appears to be a good deal slower. The results show that although the RF-ALT and DC-ALT give appreciably different lifetimes at stress conditions, they give nearly identical lifetimes at maximum recommended operating conditions. Both give over 1E6 hours at 225 °C junction temperature.

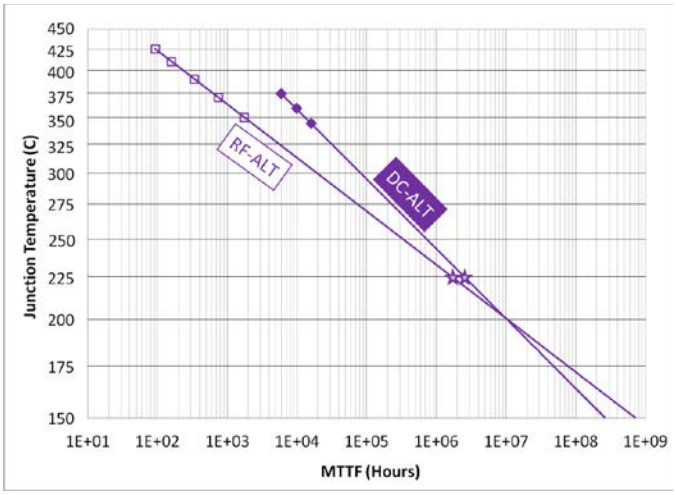


Fig. 5. Median time to failure versus junction temperature for G50V3 RF-ALT and DC-ALT. Stars represent fiducial points to illustrate the predicted lifetime at maximum rated junction temperature of 225 °C.

Visual inspection of RF-ALT failed devices showed that the devices were blown up, and could give no useful information about the failure mechanism. Visual inspection of RF-ALT devices that were stressed but not taken to failure showed voiding in the field plate metallization, as shown in Fig. 6, as confirmed by focused ion beam (FIB) cross section (not shown). The failure analysis found no evidence of ohmic contact inter-diffusion.

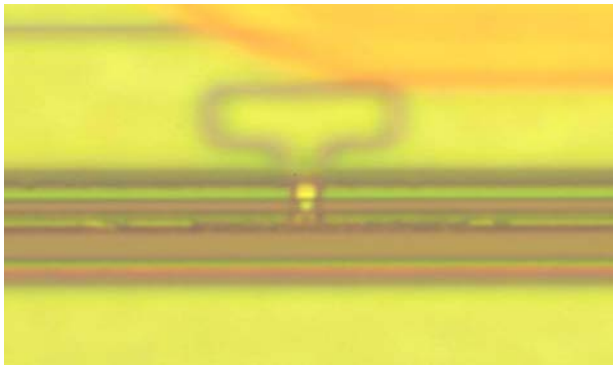

Fig. 6. Representative visual inspection image showing field plate voiding after a duration of RF-ALT stress, but prior to catastrophic failure.

Visual inspection of RF-ALT failed devices showed that the devices were blown up, and could give no useful information about the failure mechanism. Visual inspection of RF-ALT devices that were stressed but not taken to failure showed voiding in the field plate metallization. Focused ion beam (FIB) cross section showed that either voids could coalesce into larger voids inside of the passivation still intact; or, pieces of the field plate and void could pop off of the device entirely, as shown in Fig. 6. The failure analysis found no evidence of ohmic contact inter-diffusion.

Performing RF-ALT on the 28 V technologies would be a challenge, because the lower voltage means that the dissipated power during RF-ALT is considerably less, which means that much higher base plate temperatures would have to be used to reach the junction temperatures necessary to induce failures. There would be concern that secondary nuisance failure modes may be induced that would confound the result of interest. However, testing may be performed in future studies, along with careful failure analysis for determining root cause.

Previous studies have shown that for G40V4, RF-ALT and DC-ALT give comparable lifetimes for the same junction temperature [4].

### C. *Intrinsic life comparison*

Fig. 7 summarizes the intrinsic lifetime of Wolfspeed's GaN technologies. The chart represents a combination of the best ALT reliability methodologies for the corresponding technologies. The results show that although methodologies and failure modes differ, all of the technologies give high predicted lifetimes at maximum recommended junction temperatures.

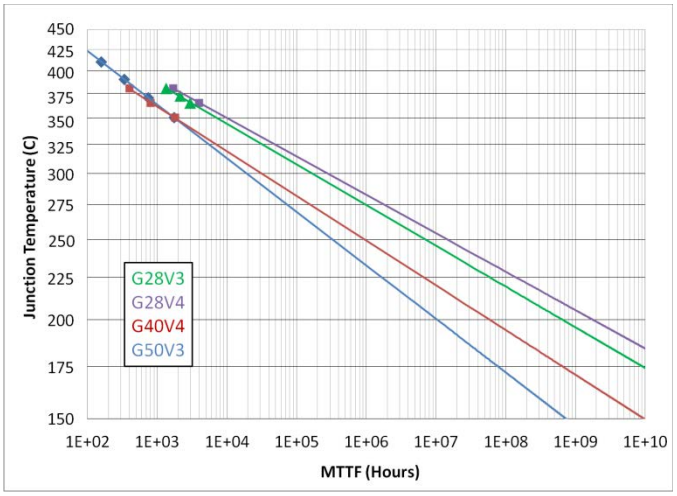


Fig. 7. Median time to failure and intrinsic lifetime extrapolations for G28V3, G28V4, and G40V4 DC-ALT, and G50V3 RF-ALT.

### D. *Qualification*

Fig. 8 summarizes the extrinsic reliability qualification results for the technologies. All qualification tests passed with zero failures.

| | | | Number of Lots * Devices = Total Sampled for Test | | | |
|---|---|---|---|---|---|---|
| **Lg (µm)** | **Tech** | **VDD** | **DC-HTOL** 225C, VDD 1000 hours | **HTRB** 150C, 2.5-3*VDD 1000 hours | **RF-HTOL** 225C, VDD 1000 hours | **TC** -65C / +150C 1000 cycles |
| 0.40 | G28 V3 | 28 V | 3*77=231<br>0 fails | 3*77=231<br>0 fails | 3*5=15<br>0 fails | 3*77=231<br>0 fails |
| | G50 V3 | 50 V | 3*40=120<br>0 fails | 3*27=81<br>0 fails | 3*3=9<br>0 fails | 3*27=81<br>0 fails |
| 0.25 | G28 V4 | 28 V | 3*25=75<br>0 fails | 3*25=75<br>0 fails | 3*5=15<br>0 fails | 3*25=75<br>0 fails |
| | G40 V4 | 40 V | 3*25=75<br>0 fails | 3*25=75<br>0 fails | 3*5=15<br>0 fails | 3*25=75<br>0 fails |

Fig. 8. Extrinsic reliability qualification results.

### E. *Field reliability*

Table 1 summarizes the current field reliability for the technologies, the first of which has been shipping commercially since 2007. The fielded device hours is calculated as: current date minus the confirmed ship date minus 90 days (allowing for time to put into service) * 12 hours per day. The FIT rate is calculated as: 2 (to allow for only half of field failures being reported) times the number of valid field failures (excludes engineering evaluations, as-received visual defect escapes or issues, as-received test escapes, packaging and assembly quality issues, and other extraneous non-Wolfspeed related issues) divided by fielded device hours; it also includes an additional factor for statistical confidence margin. The documented field failure rate is very low and on par with more established RF technologies.

TABLE I. FIELD RELIABILITY BY TECHNOLOGY

| Tech | Fielded Device Hours (Billions) | FIT Rate (valid field fails per billion device hours) |
|---|---|---|
| G28V3 | 113.3 | 0.8 |
| G50V3 | 42.3 | 0.4 |
| G40V4 | 3.2 | 1.3 |

## IV. CONCLUSION

The wear-out mechanisms have been established for the 28 V and 40 V technologies as ohmic contact degradation for 50 V technologies as field plate voiding. Intrinsic lifetime extrapolations predict high lifetimes for both mechanisms and all technologies for typical yet aggressive conditions in target applications. The technologies have been fully qualified with zero failures. The technologies have been shipping in volume since 2007 with a FIT rate of less than 2 failures per billion device hours, and volumes of over 100 billion fielded device hours.


## ACKNOWLEDGMENT

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## REFERENCES


[1] Donald A. Gajewski, Scott Sheppard, Tina McNulty, Jeff B. Barner, Jim Milligan and John Palmour, "Reliability of GaN/AlGaN HEMT MMIC Technology on 100-mm 4H-SiC," in *Reliability of Compound Semiconductors Workshop*, Indian Wells, CA, 2011.

[2] Ryan Fury et al., "GaN-on-SiC MMIC Production for S-Band and EW-Band Applications," in *The International Conference on Compound Semiconductor Manufacturing Technology*, New Orleans, LA, 2013, pp. 95-98.

[3] Simon M. Wood et al., "An Optical 0.25-µm GaN HEMT Technology on 100-mm SiC for RF Discrete and Foundry MMIC Products," in *The International Conference on Compound Semiconductor Manufacturing Technology*, New Orleans, LA, 2013, pp. 127-130.

[4] Donald A. Gajewski, Randall D. Lewis, and Benjamin Decker, "Investigation and Resolution of a Very High Ea (Threshold) Failure Mechanism in a 40V GaN FET," in *Reliability of Compound Semiconductors Workshop*, Denver, CO, 2014.

[5] Wolfspeed Application Note, "Thermal Performance Guide for High Power SiC MESFET and GaN HEMT Transistors", Available: http://www.wolfspeed.com/index.php/downloads/dl/file/id/195/product/0/thermal_performance_guide_for_high_power_sic_mesfet_and_gan_hemt_transistors.pdf

[6] Joh, J., F. Gao, T. Palacios and J. A. del Alamo, "A model for the critical voltage for electrical degradation of GaN high electron mobility transistors," in *Reliability of Compound Semiconductors Workshop*, Greensboro, NC, 2009, pp. 3-5.