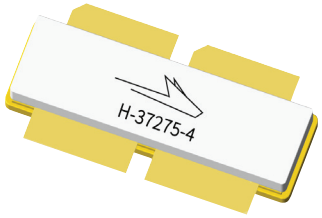
# PXAC203302FV

## Thermally-Enhanced High Power RF LDMOS FET
## 330 W, 28 V, 1880 – 2025 MHz

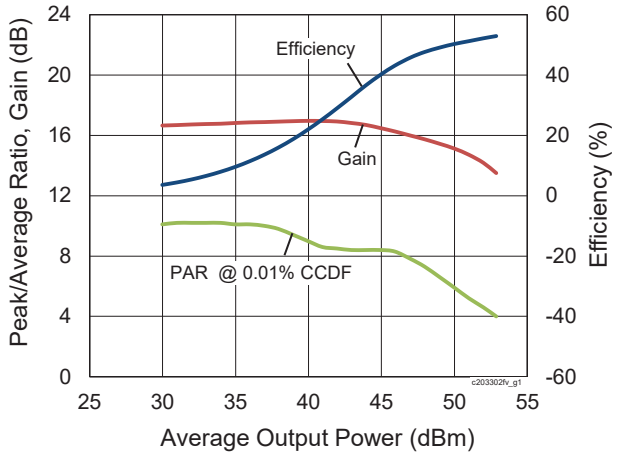
### Description

The PXAC203302FV is a 330-watt LDMOS FET with an asymmetrical design intended for use in multi-standard cellular power amplifier applications in the 1880 to 2025 MHz frequency band. Features include dual-path design, input matching, high gain and thermally-enhanced package with earless flanges. Manufactured with Wolfspeed's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.

PXAC203302FV
Package H-37275-4




**Single-carrier WCDMA Drive-up**
$V_{DD}$ = 28 V, $I_{DQ}$ = 900 mA, $f$ = 2025 MHz,
3GPP WCDMA signal,
PAR = 10 dB, 3.84 MHz BW




### Features

- Broadband internal input and output matching
- Asymmetrical Doherty design
  - Main : $P_{1dB}$ = 130 W Typ
  - Peak : $P_{1dB}$ = 200 W Typ
- Typical Pulsed CW performance, 2025 MHz, 28 V, combined outputs, Doherty Configuration
  - Output power at $P_{1dB}$ = 250 W
  - Efficiency = 55%
  - Gain = 16 dB
- Capable of handling 10:1 VSWR @28 V, 250 W (CW) output power
- Human Body Model Class 2 (per ANSI/ESDA/JEDEC JS-001)
- Integrated ESD protection
- Low thermal resistance
- Pb-free and RoHS compliant

### RF Characteristics

**Single-carrier WCDMA Specifications** (tested in Wolfspeed Doherty test fixture)
$V_{DD}$ = 28 V, $I_{DQ}$ = 900 mA, $V_{GSPEAK}$ = 1.1 V, $P_{OUT}$ = 56 W avg, $f_1$ = 2025 MHz, 3GPP signal, channel bandwidth = 3.84MHz, peak/average = 10 dB @ 0.01% CCDF

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Gain | $G_{ps}$ | 15 | 16 | — | dB |
| Drain Efficiency | $\eta_D$ | 45 | 49 | — | % |
| Adjancent Channel Power Ratio | ACPR | — | –30.5 | –26 | dBc |

*All published data at $T_{CASE}$ = 25°C unless otherwise indicated*

ESD: Electrostatic discharge sensitive device—observe handling precautions!

## DC Characteristics (each side)

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_{DS}$ = 10 mA | $V_{(BR)DSS}$ | 65 | — | — | V |
| Drain Leakage Current | $V_{DS}$ = 28 V, $V_{GS}$ = 0 V | $I_{DSS}$ | — | — | 1 | µA |
| | $V_{DS}$ = 63 V, $V_{GS}$ = 0 V | $I_{DSS}$ | — | — | 10 | µA |
| On-State Resistance (main) | $V_{GS}$ = 10 V, $V_{DS}$ = 0.1 V | $R_{DS(on)}$ | — | 0.088 | — | Ω |
| (peak) | $V_{GS}$ = 10 V, $V_{DS}$ = 0.1 V | $R_{DS(on)}$ | — | 0.088 | — | Ω |
| Operating Gate Voltage (main) | $V_{DS}$ = 28 V, $I_{DQ}$ = 900 mA | $V_{GS}$ | 2.5 | 2.7 | 2.8 | V |
| (peak) | $V_{DS}$ = 28 V, $I_{DQ}$ = 0 A | $V_{GS}$ | 0.6 | 1.1 | 1.4 | V |
| Gate Leakage Current | $V_{GS}$ = 10 V, $V_{DS}$ = 0 V | $I_{GSS}$ | — | — | 1 | µA |

## Maximum Ratings

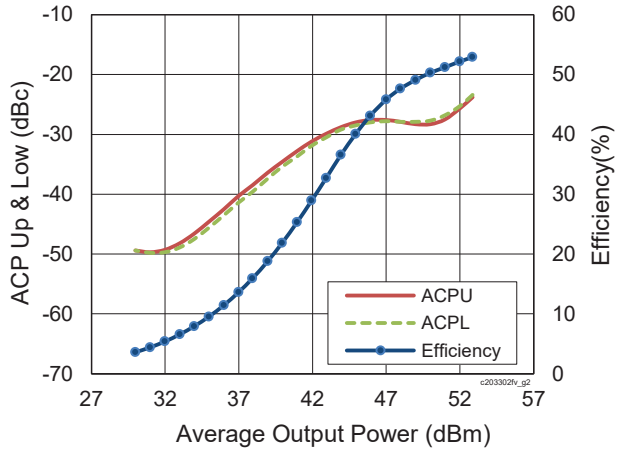
| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | 65 | V |
| Gate-Source Voltage | $V_{GS}$ | –6 to +10 | V |
| Operating Voltage | $V_{DD}$ | 0 to +32 | V |
| Junction Temperature | $T_J$ | 225 | °C |
| Storage Temperature Range | $T_{STG}$ | –65 to +150 | °C |
| Thermal Resistance (main, $T_{CASE}$ = 70°C, 56.2 W CW) | $R_{\theta JC}$ | 0.62 | °C/W |
| (peak, $T_{CASE}$ = 70°C, 260 W CW) | $R_{\theta JC}$ | 0.35 | °C/W |

## Ordering Information

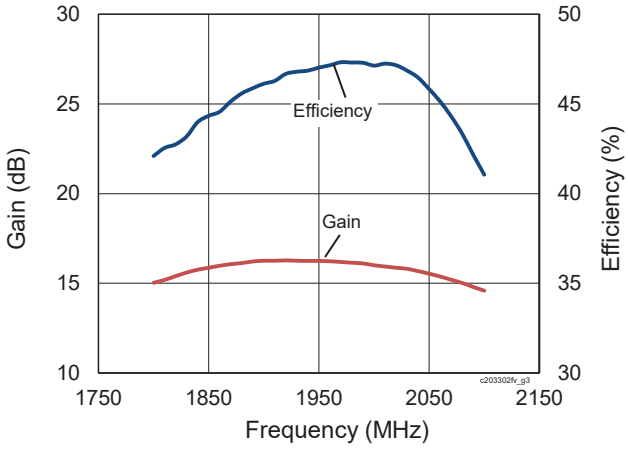
| Type and Version | Order Code | Package Description | Shipping |
|---|---|---|---|
| PXAC203302FV V1 R0 | PXAC203302FV-V1-R0 | H-37275-4, earless flange | Tape & Reel, 50 pcs |
| PXAC203302FV V1 R250 | PXAC203302FV-V1-R250 | H-37275-4, earless flange | Tape & Reel, 250 pcs |

## Typical Performance (data taken in a production test fixture)

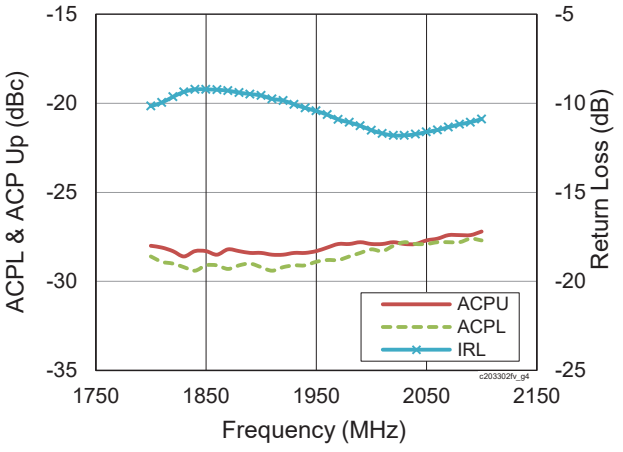
**Single-carrier WCDMA Drive-up**
$V_{DD}$ = 28 V, $I_{DQ}$ = 900 mA, $f$ = 2025 MHz,
3GPP WCDMA signal, PAR = 10 dB,
BW = 3.84 MHz



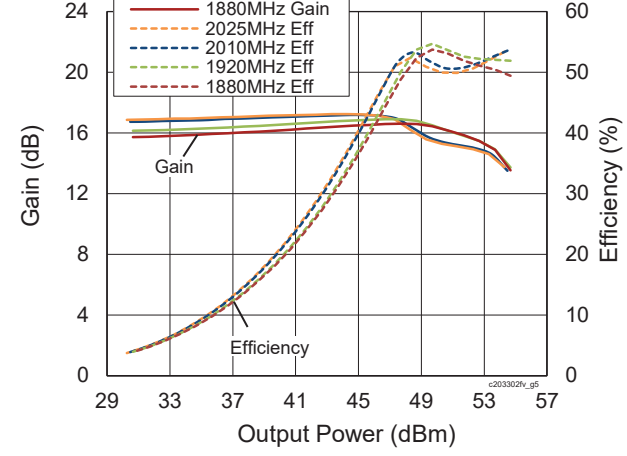

**Single-carrier WCDMA Broadband Performance**
$V_{DD}$ = 28 V, $I_{DQ}$ = 900 mA, $P_{OUT}$ = 47.5 dBm,
3GPP WCDMA signal, PAR = 10 dB



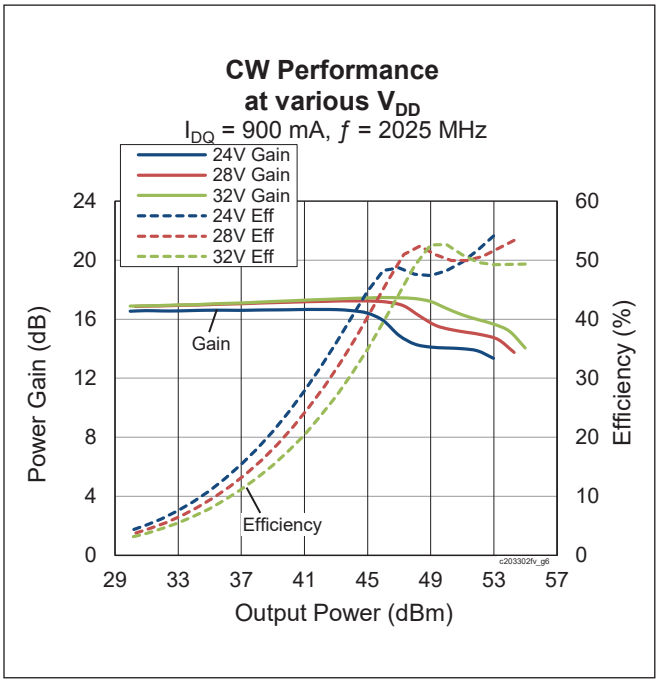

**Single-carrier WCDMA Broadband Performance**
$V_{DD}$ = 28 V, $I_{DQ}$ = 900 mA, $P_{OUT}$ = 47.5 dBm,
3GPP WCDMA signal, PAR = 10 dB

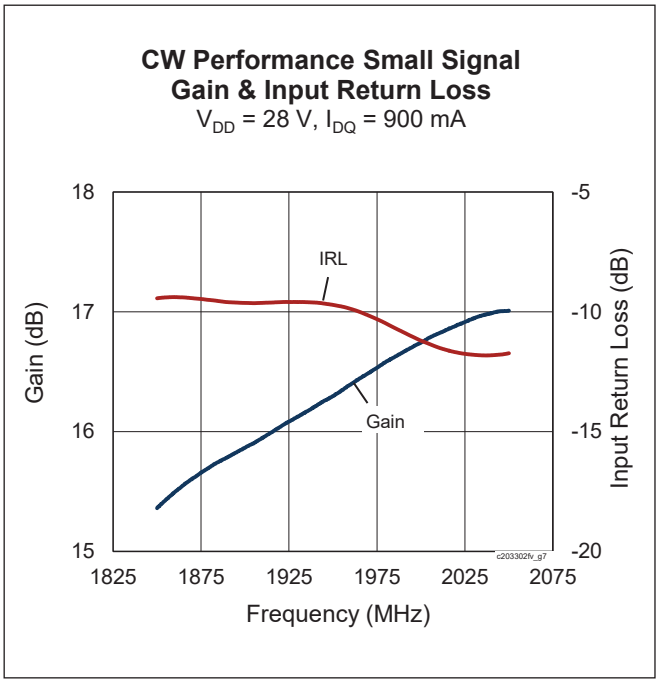



**CW Performance**
$V_{DD}$ = 28 V, $I_{DQ}$ = 900mA



## Typical Performance (cont.)




## Load Pull Performance

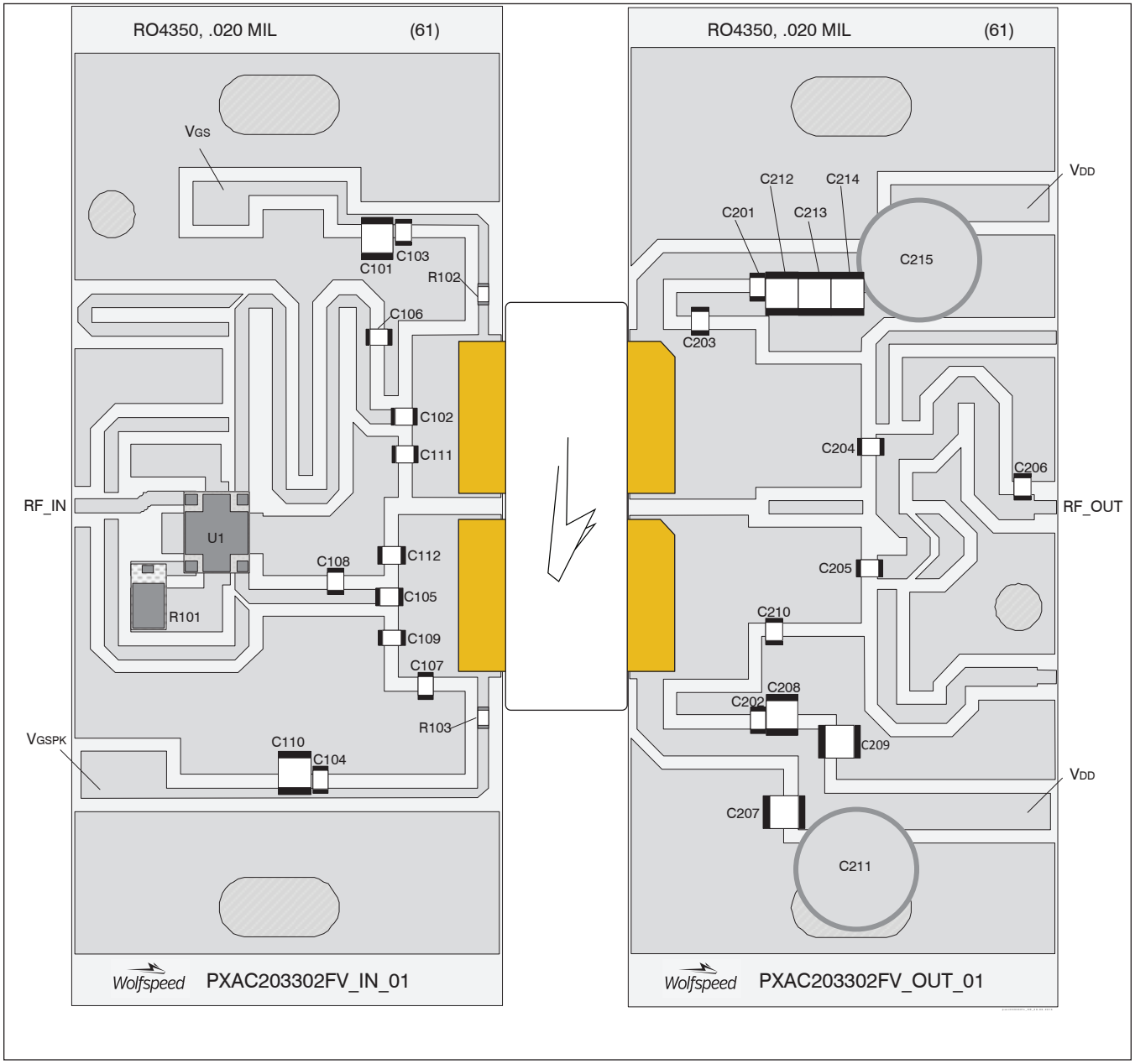
**Main Side Load Pull Performance** – Pulsed CW signal: 160 µs, 10% duty cycle, 28 V, $I_{DQ}$ = 800 mA, Class AB

| | | $P_{1dB}$ | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Max Output Power | | | | | Max Drain Efficiency | | | | |
| Freq [MHz] | Zs [Ω] | Zl [Ω] | Gain [dB] | $P_{OUT}$ [dBm] | $P_{OUT}$ [W] | $\eta_D$ [%] | Zl [Ω] | Gain [dB] | $P_{OUT}$ [dBm] | $P_{OUT}$ [W] | $\eta_D$ [%] |
| 1880 | 2.78 – j6.42 | 1.33 – j2.33 | 18.5 | 52.5 | 179 | 55.1 | 3.40 – j1.31 | 21.2 | 50.0 | 100 | 66.7 |
| 1900 | 2.94 – j6.93 | 1.31 – j2.40 | 18.5 | 52.5 | 176 | 54.4 | 2.82 – j1.21 | 21.2 | 50.1 | 102 | 65.5 |
| 1920 | 3.81 – j7.27 | 1.30 – j2.46 | 18.5 | 52.4 | 174 | 53.8 | 2.61 – j1.25 | 21.0 | 50.4 | 108 | 65.6 |
| 2010 | 6.13 – j8.11 | 1.17 – j2.61 | 18.4 | 52.1 | 164 | 50.6 | 2.19 – j1.29 | 21.2 | 50.0 | 100 | 63.2 |
| 2025 | 8.73 – j8.92 | 1.29 – j2.65 | 18.8 | 52.2 | 168 | 53.9 | 2.19 – j1.35 | 21.2 | 50.1 | 101 | 62.9 |

**Peak Side Load Pull Performance** – Pulsed CW signal: 160 µs, 10% duty cycle, 28 V, $V_{GS}$ = 1.4 V, Class C

| | | $P_{1dB}$ | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Max Output Power | | | | | Max Drain Efficiency | | | | |
| Freq [MHz] | Zs [Ω] | Zl [Ω] | Gain [dB] | $P_{OUT}$ [dBm] | $P_{OUT}$ [W] | $\eta_D$ [%] | Zl [Ω] | Gain [dB] | $P_{OUT}$ [dBm] | $P_{OUT}$ [W] | $\eta_D$ [%] |
| 1880 | 1.47 – j3.68 | 2.40 – j2.40 | 15.4 | 54.0 | 250 | 54.8 | 1.69 – j0.40 | 16.5 | 52.0 | 159 | 65.4 |
| 1900 | 1.52 – j4.02 | 2.08 – j2.31 | 15.8 | 54.0 | 249 | 55.8 | 1.58 – j0.55 | 16.9 | 52.1 | 164 | 66.9 |
| 1920 | 1.54 – j4.21 | 2.29 – j2.39 | 15.9 | 53.9 | 247 | 55.6 | 1.44 – j0.58 | 17.0 | 51.9 | 156 | 66.7 |
| 2010 | 2.84 – j4.51 | 2.51 – j2.67 | 16.1 | 53.7 | 236 | 54.5 | 1.50 – j1.19 | 17.2 | 52.1 | 162 | 64.3 |
| 2025 | 4.34 – j5.13 | 2.68 – j2.58 | 16.4 | 53.8 | 192 | 55.2 | 1.37 – j1.22 | 17.3 | 51.9 | 155 | 64.6 |

## Reference Circuit , 1880 – 2025 MHz




*Reference circuit assembly diagram (not to scale)*

## Reference Circuit (cont.)

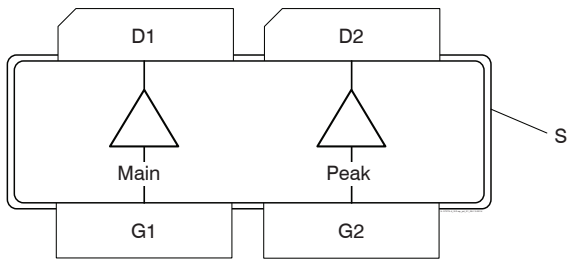
### Reference Circuit Assembly

| | |
|---|---|
| DUT | PXAC203302FV-V1 |
| Test Fixture Part No. | LTA/PXAC203302FV-V1 |
| PCB | Rogers 4350, 0.508 mm [0.020"] thick, 2 oz. copper, $\varepsilon_r$ = 3.66, $f$ = 1880 – 2025 MHz |
| Find Gerber files for this test fixture on the Wolfspeed Web site at http://www.wolfspeed.com/RF | |

### Components Information

| Component | Description | Manufacturer | P/N |
|---|---|---|---|
| **Input** | | | |
| C101, C110 | Capacitor, 10 µF | Taiyo Yuden | UMK325C7106MM-T |
| C102, C103, C104, C105 | Capacitor, 15 pF | ATC | ATC600F150JT250XT |
| C106, C111 | Capacitor, 1 pF | ATC | ATC600F1R0BT250XT |
| C107 | Capacitor, 2.7 pF | ATC | ATC600F2R7BT250XT |
| C108 | Capacitor, 1.6 pF | ATC | ATC600F1R6BT250XT |
| C109 | Capacitor, 0.5 pF | ATC | ATC600F0R5BT250XT |
| C112 | Capacitor, 0.8 pF | ATC | ATC600F0R8BT250XT |
| R101, R102 | Resistor, 10 Ω | Panasonic Electronic Components | ERJ-3GEYJ100V |
| R103 | Resistor, 50 Ω | Richardson | C16A50Z4 |
| U1 | Hybrid Coupler | Anaren | X3C19P1-05S |
| **Output** | | | |
| C201, C202 | Capacitor, 15 pF | ATC | ATC600F150JT250XT |
| C203 | Capacitor, 1.6 pF | ATC | ATC600F1R6BT250XT |
| C204, C205 | Capacitor, 6.8 pF | ATC | ATC600F6R8BT250XT |
| C206 | Capacitor, 0.3 pF | ATC | ATC600F0R3BT250XT |
| C207, C208, C209, C212, C213, C214 | Capacitor, 10 µF | Taiyo Yuden | UMK325C7106MM-T |
| C210 | Capacitor, 0.5 pF | ATC | ATC600F0R5BT250XT |
| C211, C215 | Capacitor, 220 µF | Cornell Dubilier Electronics (CDE) | SK221M050ST |

## Pinout Diagram (top view)




| Pin | Description |
|---|---|
| D1 | Drain device 1 (Main) |
| D2 | Drain device 2 (Peak) |
| G1 | Gate device 1 (Main) |
| G2 | Gate device 2 (Peak) |
| S | Source (flange) |

*Lead connections for PXAC203302FV*

## Package Outline Specifications

### Package H-37275-4

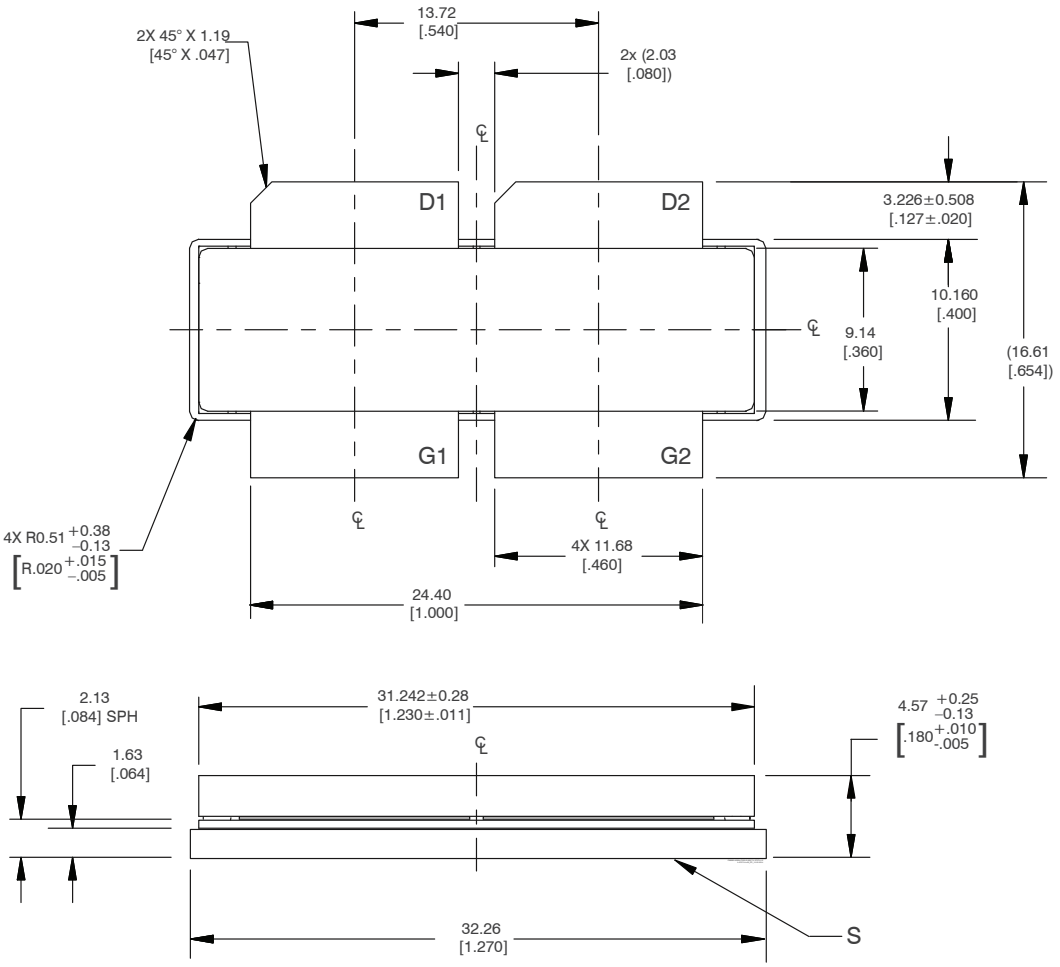



Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [.005] unless specified otherwise.
4. Pins: D1, D2 – drains; G1, G2 – gates; S – source.
5. Lead thickness: 0.127 + 0.051 mm [0.005 ± 0.002 inch].
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch].

## Revision History

| Revision | Date | Data Sheet Type | Page | Subjects (major changes since last revision) |
|---|---|---|---|---|
| 01 | 2014-03-03 | Advance | All | Proposed specification for new product development. |
| 02 | 2014-06-12 | Production | All | Specification for production-released device. |
| 02.1 | 2014-06-30 | Production | 1 | Corrected typo in features. |
| 02.2 | 2016-06-22 | Production | 2 | Updated ordering information |
| 03 | 2018-07-02 | Production | All | Converted to Wolfspeed Data Sheet |
| 03.1 | 2018-11-08 | Production | 6 | Corrected test fixture part no. |

For more information, please contact:

4600 Silicon Drive
Durham, North Carolina, USA 27703
www.wolfspeed.com/RF

Sales Contact
RFSales@wolfspeed.com

RF Product Marketing Contact
RFMarketing@wolfspeed.com
919.407.7816

## Notes

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