CPM2-1200-0160B

Silicon Carbide Power MOSFET
C2M™ MOSFET Technology

N-Channel Enhancement Mode

V_{DS}	1200 V
I_D @ 25˚C	19 A
$R_{DS(on)}$	160 mΩ

Features

- New C2M SiC MOSFET technlogy
- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Avalanche Ruggedness
- Resistant to Latch-Up
- Halogen Free, RoHS Compliant

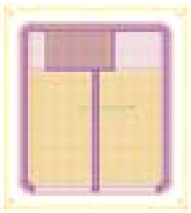
Benefits

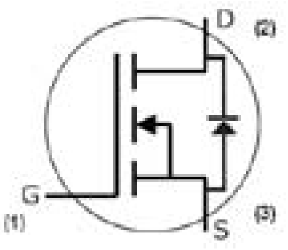
- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

Applications

- Solar Inverters
- Switch Mode Power Supplies
- High Voltage DC/DC Converters
- LED Lighting Power Supplies

Chip Outline





Part Number	Die Size (mm)
CPM2-1200-0160B	2.39 × 2.63

Maximum Ratings (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1200	V	V_{GS} = 0 V, I_D = 100 μA	
V_{GSmax}	Gate - Source Voltage	-10/+25	V	Absolute maximum values	
V_{GSop}	Gate - Source Voltage	-5/+20	V	Recommended operational values	
I_D	Continuous Drain Current	19	A	V_{GS} = 20 V, T_C = 25˚C	
		12.5		V_{GS} = 20 V, T_C = 100˚C	
$I_{D(pulse)}$	Pulsed Drain Current	40	A	Pulse width t_P limited by T_{jmax}	
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +150	˚C		
T_L	Solder Temperature	260	˚C	1.6mm (0.063") from case for 10s	
T_{Proc}	Maximum Processing Temperature	325	˚C	10 min. maximum	

Note (1): Assumes a $R_{\theta JC}$ < 0.90 K/W

Electrical Characteristics (T$_C$ = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D = 100 μA	
$V_{GS(th)}$	Gate Threshold Voltage	2.4	2.5		V	V_{DS} = 10V, I_{DS} = 2.5 mA	Fig. 11
		1.8	1.9		V	V_{DS} = 10V, I_{DS} = 2.5 mA, T_J = 150ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	100	μA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current			250	nA	V_{GS} = 20 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		160	196	mΩ	V_{GS} = 20 V, I_D = 10 A	Fig. 4, 5, 6
			290			V_{GS} = 20 V, I_D = 10A, T_J = 150ºC	
g_{fs}	Transconductance		4.8		S	V_{DS}= 20 V, I_{DS}= 10 A	Fig. 7
			4.3			V_{DS}= 20 V, I_{DS}= 10 A, T_J = 150ºC	
C_{iss}	Input Capacitance		525		pF	V_{GS} = 0 V V_{DS} = 1000 V f = 1 MHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		47				
C_{rss}	Reverse Transfer Capacitance		4				
E_{oss}	C_{oss} Stored Energy		25		μJ		Fig. 16
E_{AS}	Avalanche Energy, Single Pluse		600		mJ	I_D = 10A, V_{DD} = 50V	
E_{ON}	Turn-On Switching Energy		79		μJ	V_{DS} = 800 V, V_{GS} = -5/20 V, I_D = 10A, $R_{G(ext)}$ = 2.5Ω, L= 256 μH	
E_{OFF}	Turn Off Switching Energy		57				
$t_{d(on)}$	Turn-On Delay Time		9		ns	V_{DD} = 800 V, V_{GS} = -5/20 V I_D = 10 A $R_{G(ext)}$ = 2.5 Ω, R_L = 80 Ω Timing relative to V_{DS} Per IEC60747-8-4 pg 83	
t_r	Rise Time		11				
$t_{d(off)}$	Turn-Off Delay Time		16				
t_f	Fall Time		10				
$R_{G(int)}$	Internal Gate Resistance		6.5		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		7		nC	V_{DS} = 800 V, V_{GS} = -5/20 V I_D = 10 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		14				
Q_g	Total Gate Charge		34				

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	3.3		V	V_{GS} = -5 V, I_F=5 A	Fig. 8,9, 10
		3.1			V_{GS} = -5V, I_F=5 A, T_J = 150 ºC	
I_S	Continuous Diode Forward Current		19	A	T_C = 25°C	Note 2
t_{rr}	Reverse Recovery Time	23		ns	V_{GS} = - 5 V, I_{SD} = 10 A, V_R = 800 V dif/dt = 3200 A/μs	Note 2
Q_{rr}	Reverse Recovery Charge	105		nC		
I_{rrm}	Peak Reverse Recovery Current	9		A		

Note (2): When using SiC Body Diode the maximum recommended V_{GS} = -5V

Note (3): For inductive and resistive switching data and waveforms please refer to datasheet for packaged device. Part number C2M0160120D.

Typical Performance

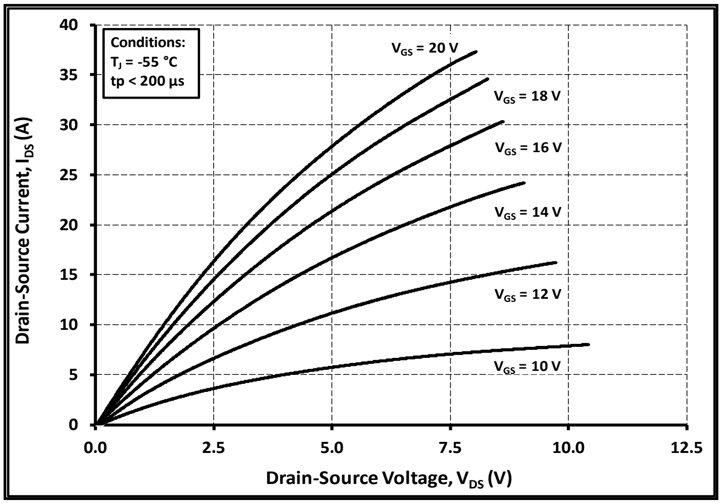


Figure 1. Output Characteristics T_J = -55 ºC

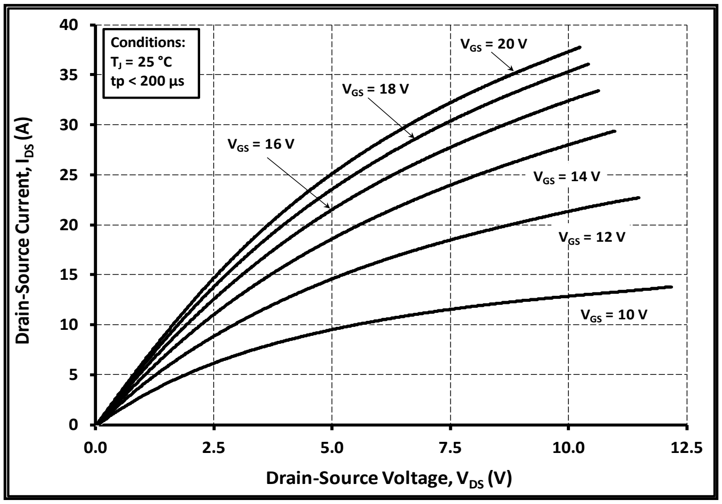


Figure 2. Output Characteristics T_J = 25 ºC

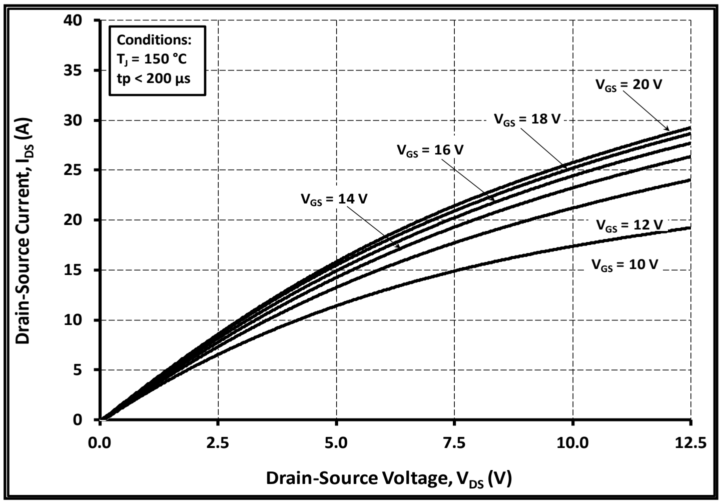


Figure 3. Output Characteristics T_J = 150 ºC

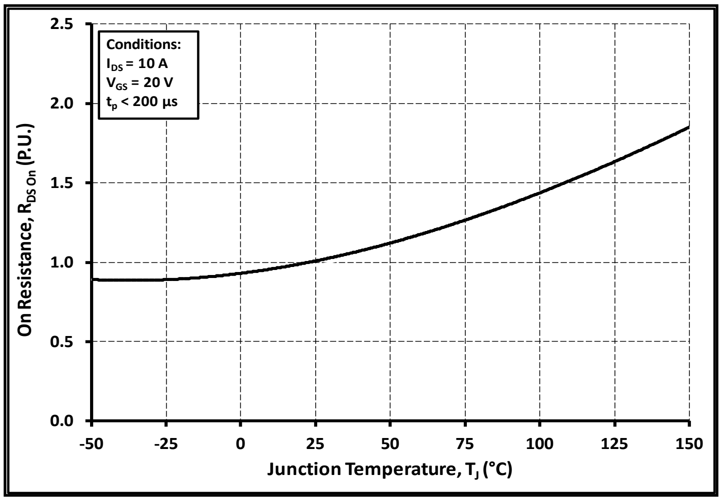


Figure 4. Normalized On-Resistance vs. Temperature

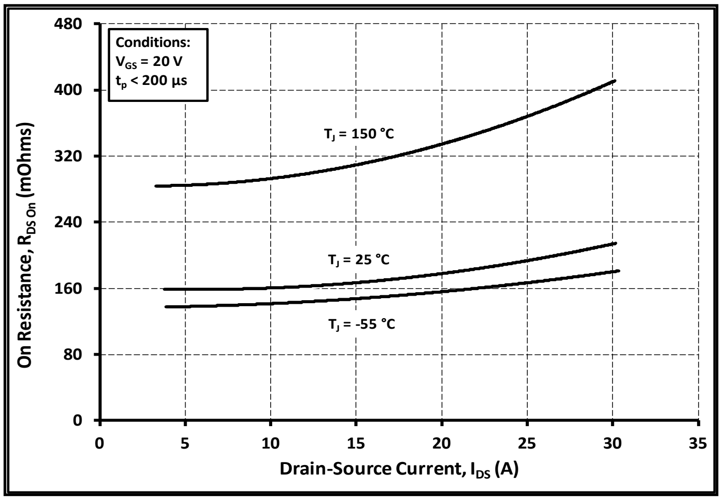


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

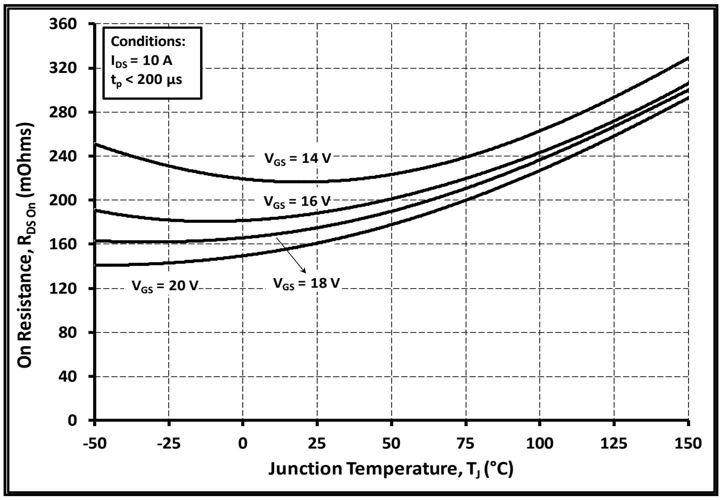


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

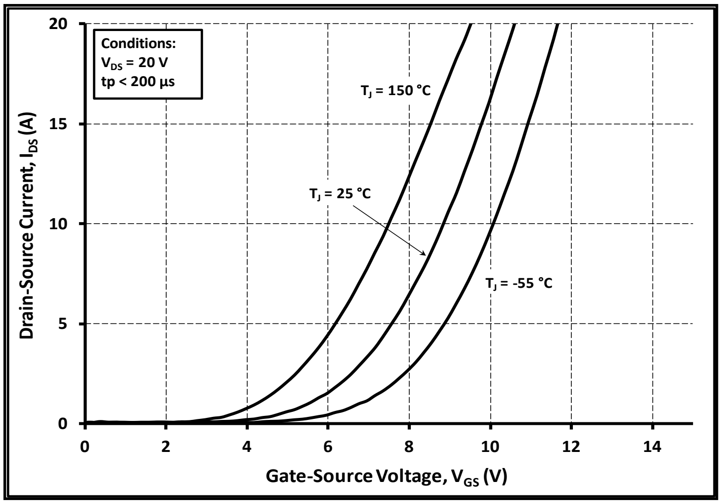


Figure 7. Transfer Characteristic for Various Junction Temperatures

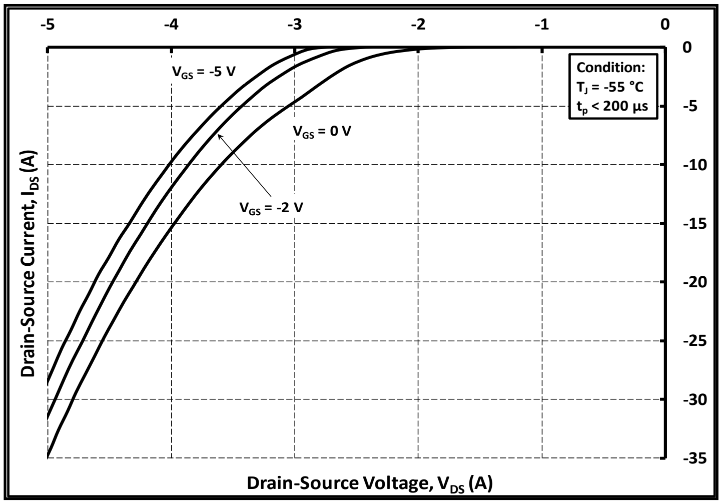


Figure 8. Body Diode Characteristic at -55 ºC

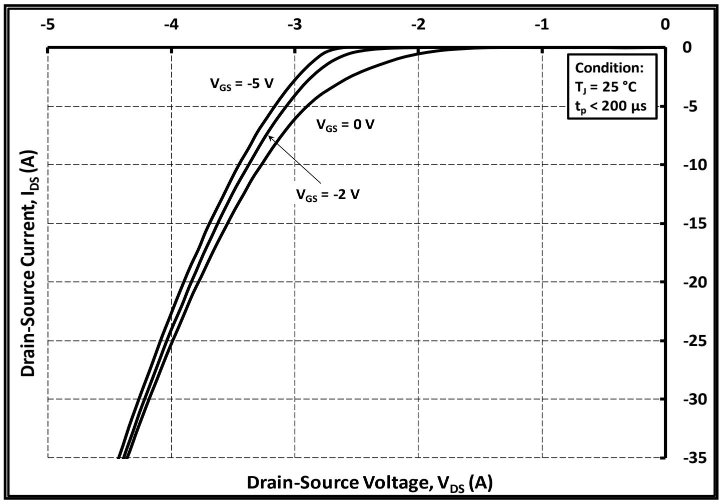


Figure 9. Body Diode Characteristic at 25 ºC

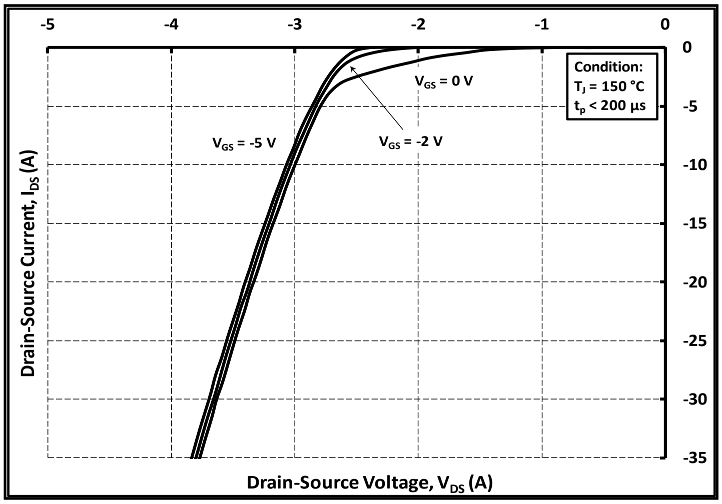


Figure 10. Body Diode Characteristic at 150 ºC

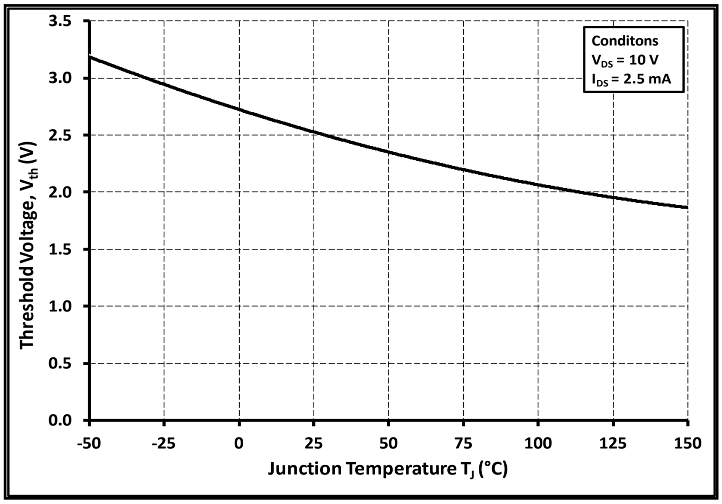


Figure 11. Threshold Voltage vs. Temperature

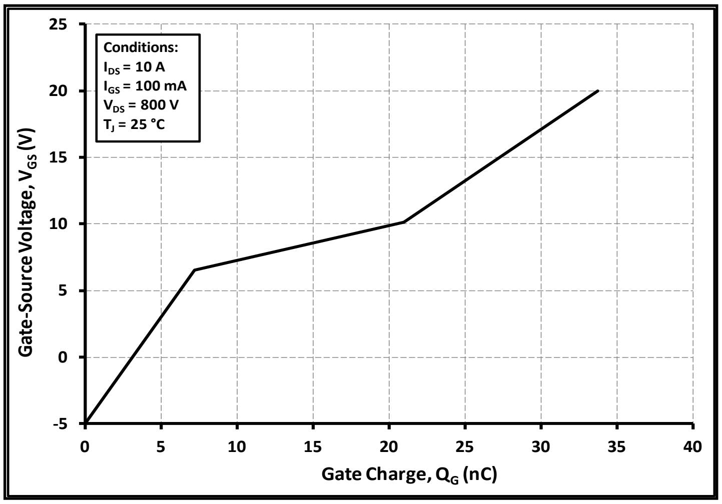


Figure 12. Gate Charge Characteristics

Typical Performance

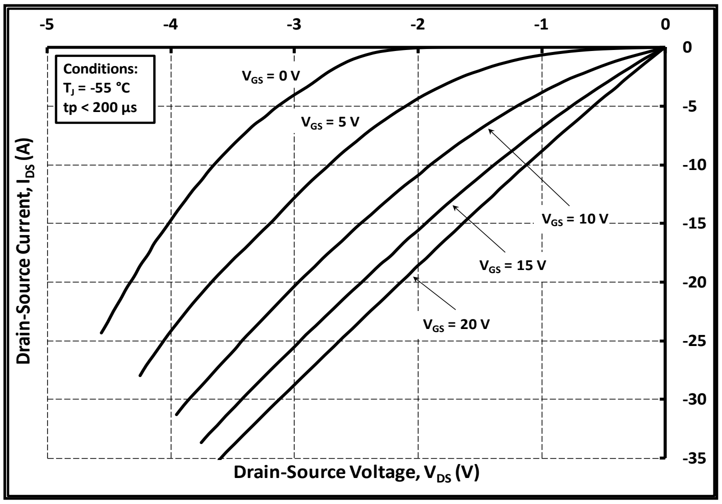


Figure 13. 3rd Quadrant Characteristic at -55 ºC

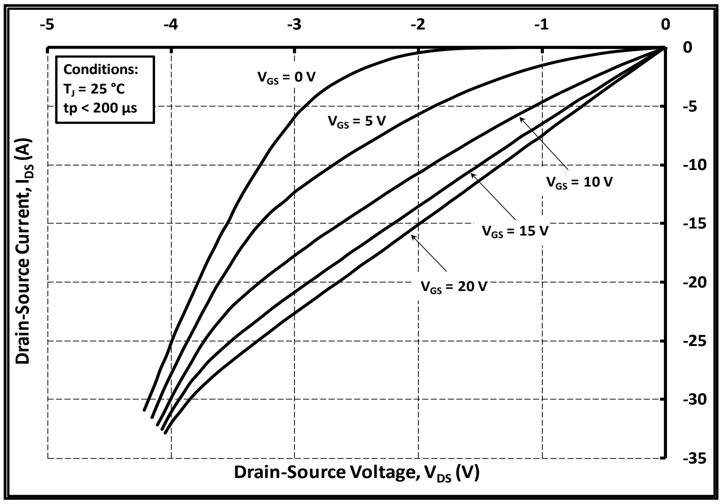


Figure 14. 3rd Quadrant Characteristic at 25 ºC

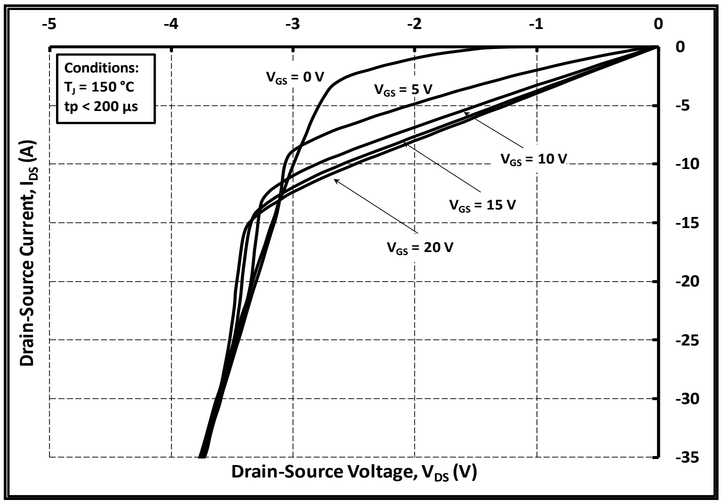


Figure 15. 3rd Quadrant Characteristic at 150 ºC

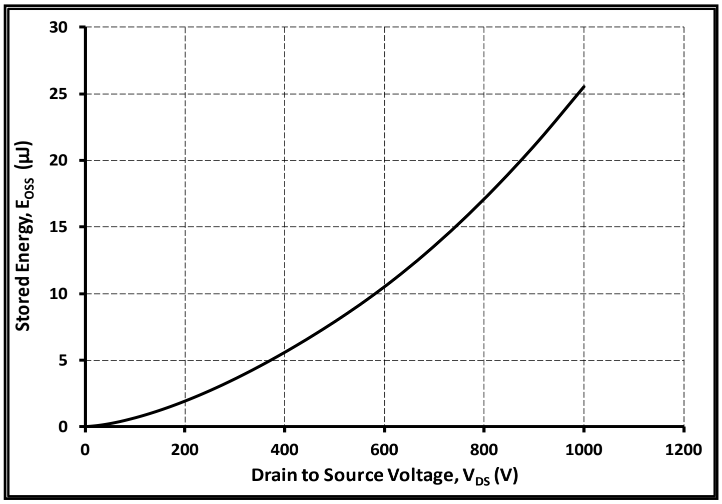


Figure 16. Output Capacitor Stored Energy

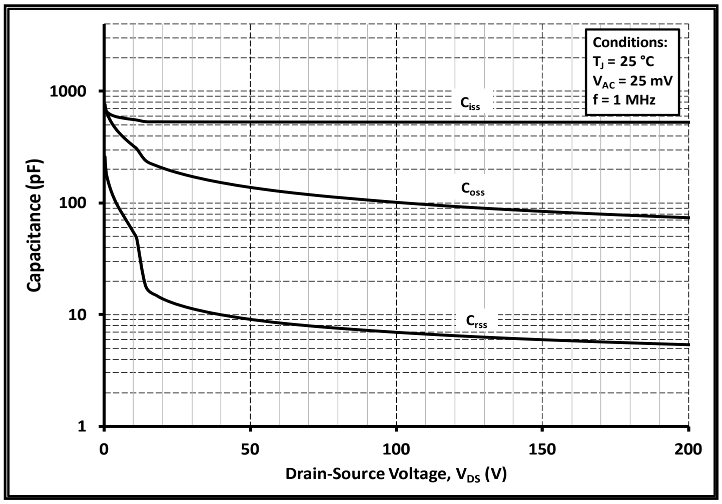


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

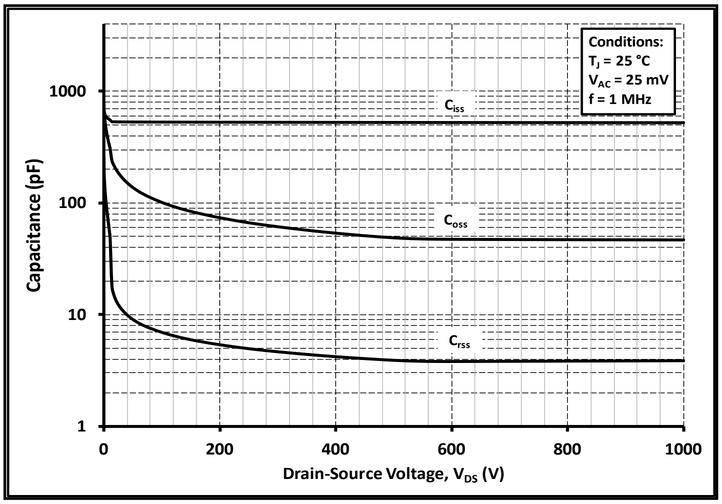
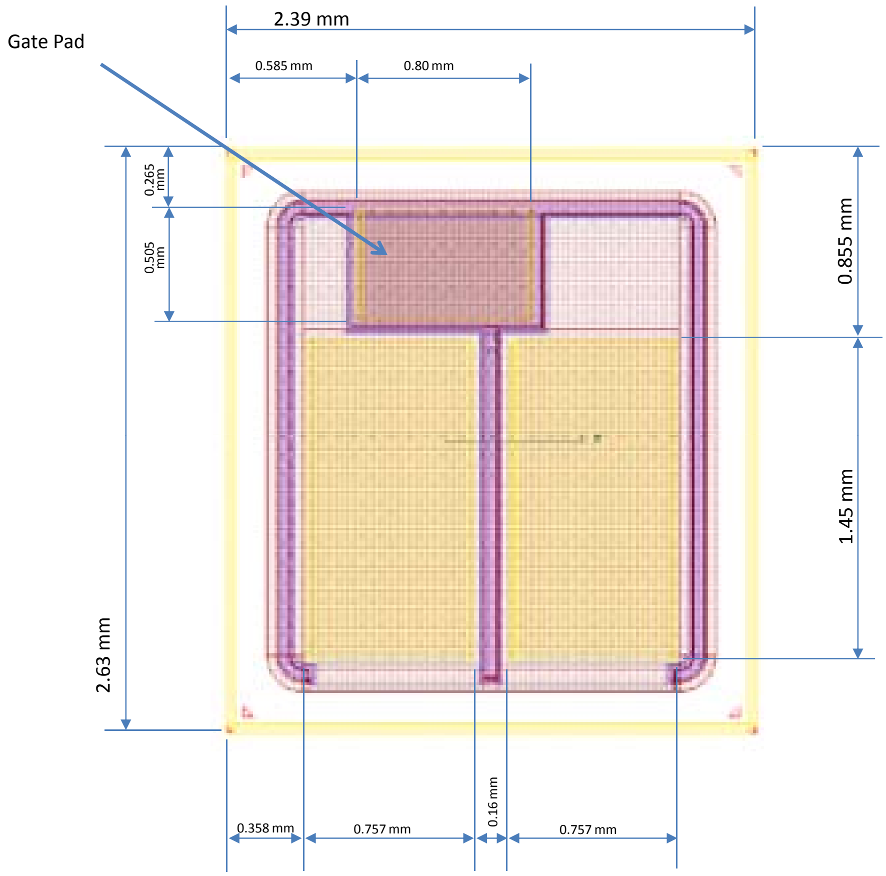


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1000V)

Mechanical Parameters

Parameter	Typical Value	Unit
Die Dimensions (L x W)	2.39 × 2.63	mm
Exposed Source Pad Metal Dimensions (LxW) Each	0.757 × 1.45	mm
Gate Pad Dimensions (L x W)	0.80 × 0.505	mm
Die Thickness	180 ± 40	µm
Top Side Source metallization (Al)	4	µm
Top Side Gate metallization (Al)	4	µm
Bottom Drain metallization (Ni/Ag)	0.8 / 0.6	µm

Chip Dimensions



Notes

- **RoHS Compliance**
  The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of www.cree.com.

- **REACh Compliance**
  REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future,please contact a Cree representative to insure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.

Related Links

- **C2M PSPICE Models: www.cree.com/power**
- **SiC MOSFET Isolated Gate Driver reference design: www.cree.com/power**
- **Application Considerations for Silicon-Carbide MOSFETs: www.cree.com/power**

Cree, Inc.
4600 Silicon Drive
Durham, NC 27703
USA Tel: +1.919.313.5300
Fax: +1.919.313.5451
www.cree.com/power