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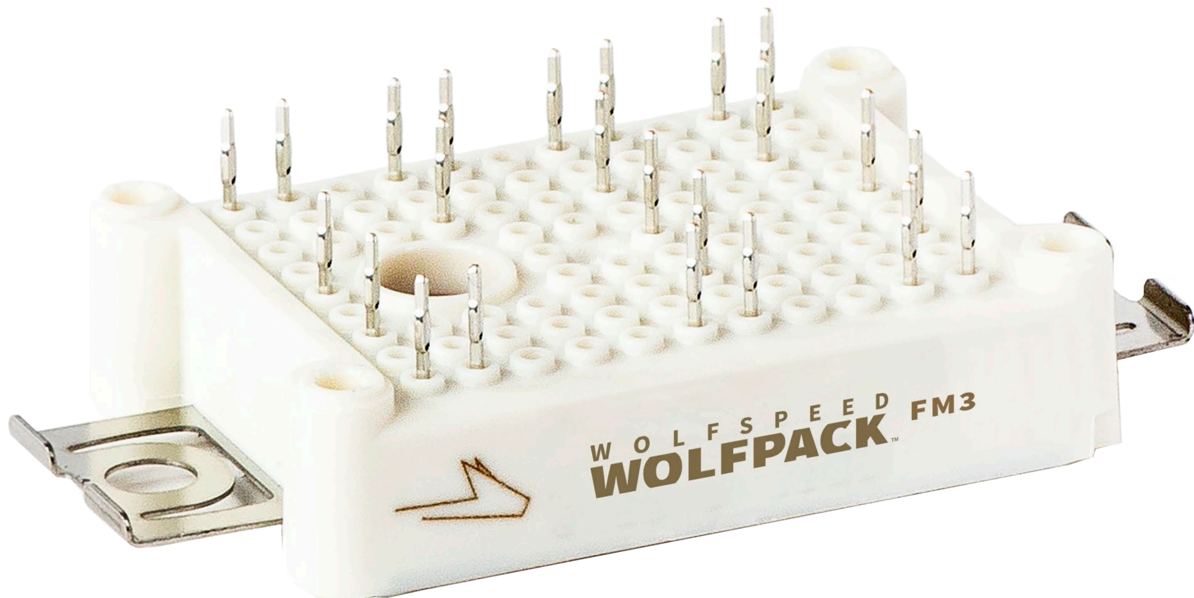
Application Note **PRD-07968**

Wolfspeed WolfPACK™ Dynamic Performance



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Double-pulse testing is a useful tool for evaluating the dynamic performance of Wolfspeed WolfPACK™ power modules. However, extracting useful and accurate results requires careful attention to layout and metrology. This document provides recommendations and guidance for designing the necessary hardware for performing double-pulse tests on WolfPACK power modules. The recommended configuration is then used to evaluate the dynamic performance of a CAB011M12FM3 power module.

CONTENTS

1. Introduction 3
2. Hardware Overview 3
   2.1. Module Overview 3
   2.2. CIL Evaluation Kit 4
   2.3. Characterization of Switching Losses 5
   2.4. Characterization of Reverse Recovery Losses 6
   2.5. Probe Recommendations 7
      2.5.1. Current Measurement 7
      2.5.2. Drain Voltage Measurement 9
      2.5.3. High-Side Gate Measurements 10
3. Design Guidance for Optimal Dynamic Performance 11
   3.1. Power Loop Layout Recommendations 12
   3.2. Gate Loop Layout Recommendations 14
   3.3. General Module Performance 15
   3.4. Selection of Gate Resistor 17
   3.5. Gate Driving Options 19

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1. Introduction

This document focuses on the **CAB011M12FM3** high performance, half-bridge module. The module features Wolfspeed® C3M™ silicon carbide (SiC) MOSFETs and is part of the flexible Wolfspeed WolfPACK™ Power Modules family. These modules eliminate the traditional baseplate for improved thermal performance. Additionally, the pin grid design allows for scalability and flexibility, with many module options in the same standard housing. This allows development of alternate converter configurations and topologies with minimal changes to thermal management systems and electrical design.

2. Hardware Overview

2.1 Module Overview

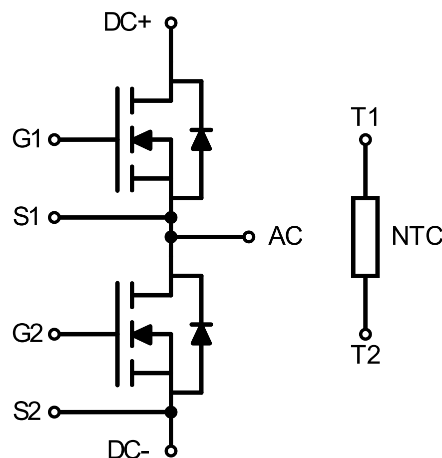

Figure 1. CAB011M12FM3 (half-bridge) module schematic

As shown by Figure 1, the CAB011M12FM3 is a half-bridge module with internal negative temperature coefficient (NTC) thermistor. The module does not contain external diodes, the diodes pictured are the body-diodes of the SiC MOSFETs.

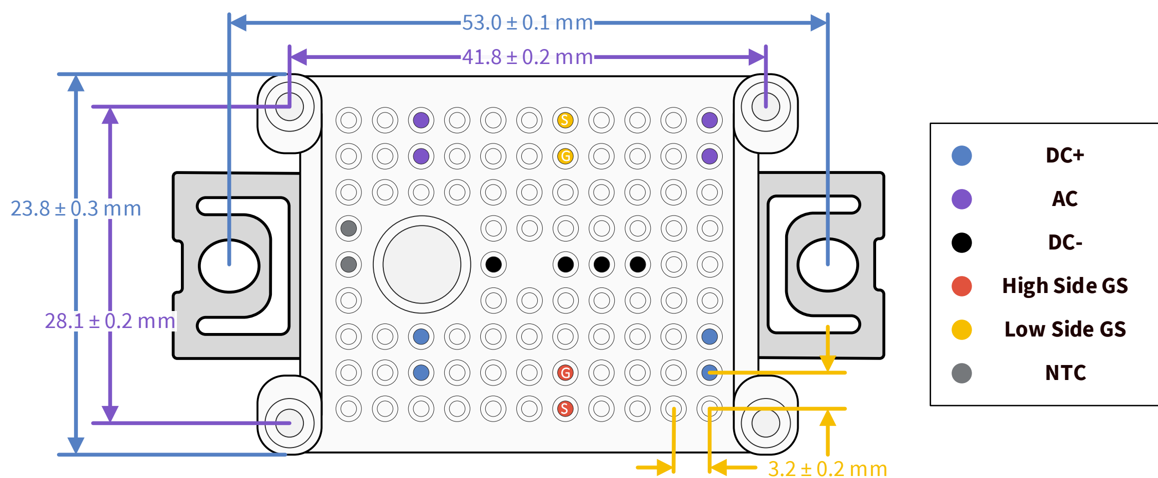

Figure 2. Layout of module pins

Figure 2 shows the pinout and dimensions of the module. Additional information can be found in the datasheet.

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2.2 CIL Evaluation Kit

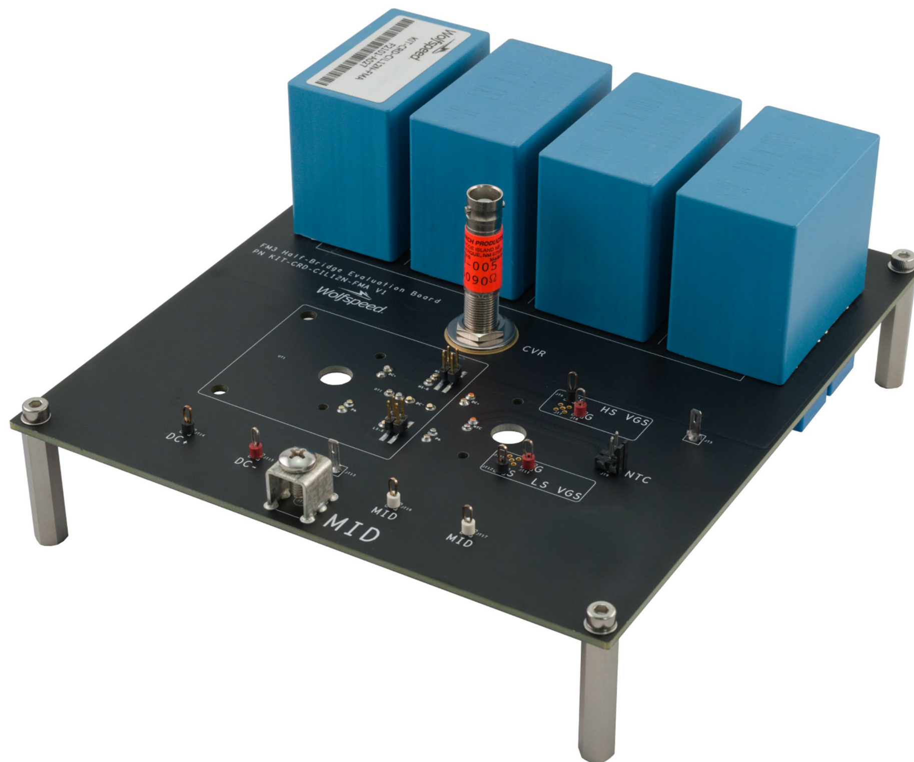

Figure 3. CIL evaluation kit for FM3 module

The CIL evaluation kit, shown in Figure 3, is available for dynamic evaluation of the power module and used to create the time domain data in this document.

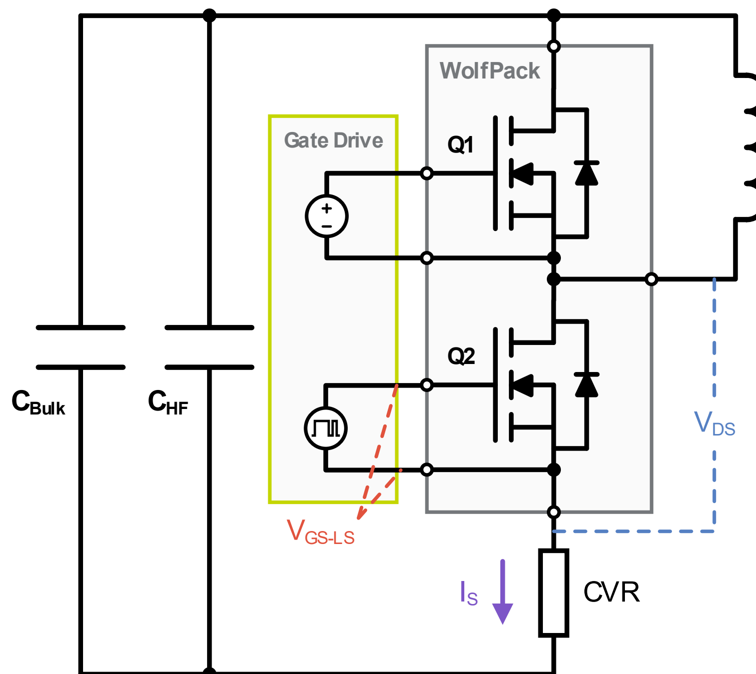

Figure 4. CIL schematic, setup for forward switching characterization

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The schematic of the CIL evaluation kit is shown in Figure 4, configured for characterization of Q2's forward dynamic behavior. The low-side device, Q2, is actively gated while the high-side device, Q1, is biased off. Current is measured with a current viewing resistor (CVR) and a high-voltage probe measures the switching voltage across low-side switch's drain to source pins. The bulk and high frequency capacitors are located on the CIL evaluation board PCB, but the load inductor is offboard and connects to the screw terminals. Two different types of capacitors are utilized to serve different functions. The bulk capacitors located on top of the board serve to provide energy storage for the system. This allows the user to utilize relays/contactors to charge the system up, then physically isolate the power supply from the system and utilize the single ground of the CVR. The capacitors have enough energy storage to provide the inductor current to exercise the system. Smaller, high frequency capacitors are located on the bottom side of the board underneath the bulk capacitors. These capacitors have much less capacitance but are also physically much smaller in size and therefore have much lower stray inductance. These capacitors serve to minimize the stray inductance of the system at higher frequencies where fast edge rates can cause high di/dt. Without these smaller, lower inductance capacitors, more voltage overshoot will be observed. Low inductance capacitors are always recommended to minimize stray inductance in the commutation loop, however, if these are not permissible for the end application, the CIL evaluation kit can be modified and these capacitors can be removed to determine expected behavior with higher stray inductance.

2.3 Characterization of Switching Losses

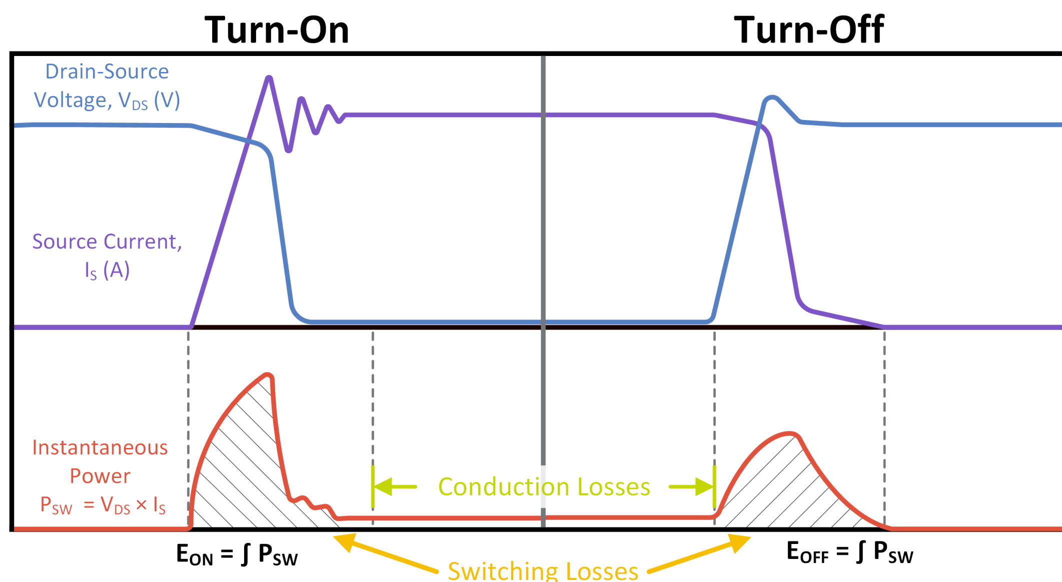

Figure 5. Notional waveforms, forward switching of Q2

Figure 5 shows notional waveforms for Q2 when actively switched, assuming current is flowing through the load inductor. The first transition of Figure 5 shows turn-on. Prior to this event, current is already commutation from the load inductor through the body diode of the high-side switch, Q1. Once the gate voltage of Q2 reaches threshold, current will begin commutating from the capacitors, through the load inductor and through Q2. The transition is seen in the rising source current, which will increase until the device is conducting the full load inductor current. During this time, the voltage drop across the device is much higher than $R_{DS(ON)} * I_S$, and the

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instantaneous power loss in this window is a major contributor to switching losses. Finally, the device current will overshoot beyond the nominal inductor current, but this event is of minimal significance compared to voltage overshoot.

Figure 5 shows notional waveforms of Q2 during the turn-off transient event. Once gate voltage falls below threshold, the voltage across Q2 will begin to rise as the channel current decreases. As the voltage rises, an additional voltage is induced by the changing current in the parasitic inductance of the circuit. This leads to a voltage overshoot at turn-off, which is dependent on switch current (I_S), device slew rate (controlled by the gate resistor), and parasitic inductance in the circuit. High voltage overshoot events can lead to device degradation, reduced lifetime, or instantaneous failure. Selection of the turn-off gate resistance should be carefully selected to balance efficiency against reliability. More detail on gate resistor selection is given in Section 3.4.

2.4 Characterization of Reverse Recovery Losses

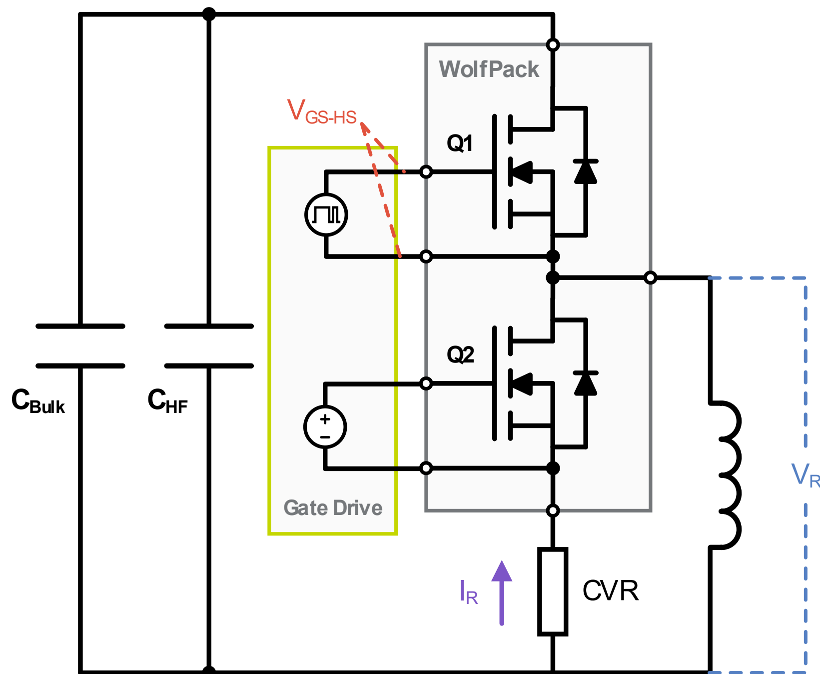

Figure 6. CIL schematic, setup for reverse recovery characterization of Q2's body diode

In addition to active switching events, forced commutated events can also be characterized using the CIL evaluation kit. Figure 6 shows the forced commutation configuration; by altering the load configuration and actively gating the high-side switch, Q1, the body diode of the low-side switch, Q2, can be evaluated. Q2 is biased off by the gate drive in these tests.

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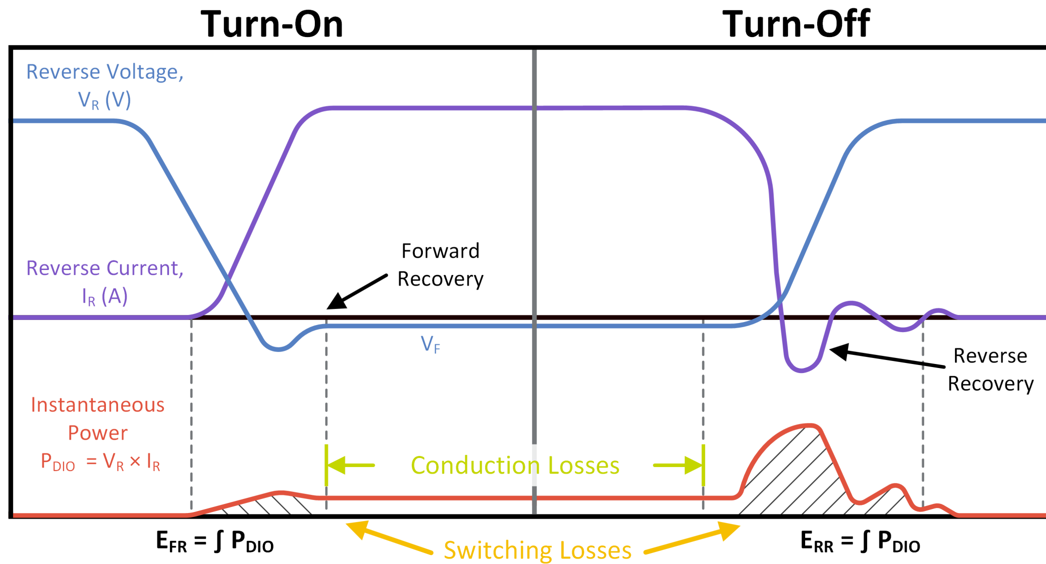

Figure 7. Notional waveforms, reverse recovery

Figure 7 shows notional transient waveforms for the body diode of Q2 at turn-on and turn-off. The forward recovery losses are generally much smaller than the reverse recovery losses and are often ignored. Depending on device temperature and current, the reverse recover losses at turn-off may be comparable to the losses of the active switch. Due to the forward voltage of the body diode, the conduction losses of the inactive switch can be significant. Actively switching both positions asynchronously can greatly reduce this source of losses.

2.5 Probe Recommendations

The accuracy of time domain measurements, and switching loss calculations, is influenced by the accuracy and bandwidth of the probes use to collect the measurements. Several comparisons are shown between common instrument probes. While this discussion emphasizes the difference between oscilloscope probes, implementation (such as layout, parasitics, and coupling) also play a critical role in measurement accuracy.

2.5.1 Current Measurement

Figure 8. Probe examples, (a) current viewing resistor (T & M Research SSDN-005, 400 MHz), (b) Rogowski current probe (PEM CWTUM/3/B, 30 MHz)

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Two common methods for current measurement in power electronics systems are the current viewing resistor (CVR) and the Rogowski coil. The Rogowski coil is a popular choice since it can easily be added to a circuit and is a non-invasive measurement. However, such probes often have significant bandwidth limitations which make them unsuitable for use with SiC. CVRs, on the other hand, have extremely high bandwidth and can be used to make accurate current measurements. Unfortunately, the need to add an additional component in series to the transistor requires careful planning during PCB layout, and the addition of a CVR will generally increase parasitic inductance in the circuit.

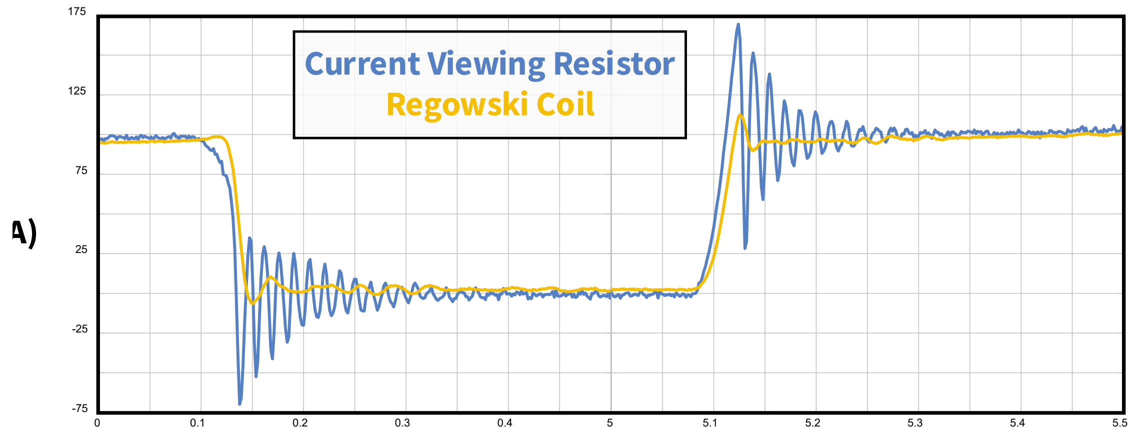

Figure 9. CVR vs Rogowski current probe, CAB016M12FM3 (T_J = 25°C, R_G = 6.8 Ω, V_{DS} = 600 V, I_S = 100 A)

Figure 9 shows a comparison of the Rogowski coil and CVR for a typical SiC hard switching event. The substantially lower bandwidth of the Rogowski coil leads to an artificial suppression of the ringing present in the experimental waveform. More importantly, it artificially suppresses the initial overshoot and alters the di/dt of the measurement.

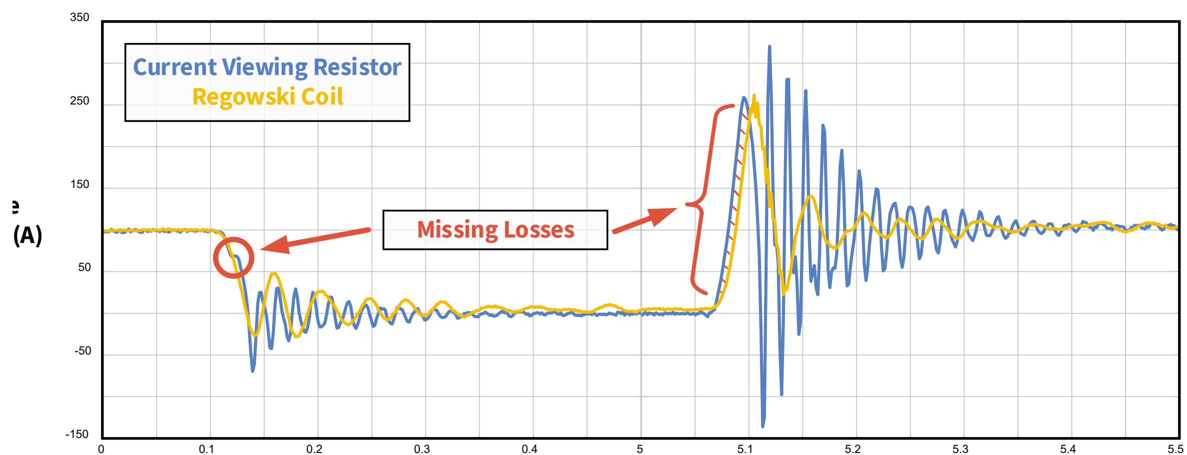

Figure 10. CVR vs Rogowski current probe, CAB011M12FM3 (T_J = 150°C, R_G = 1 Ω, V_{DS} = 600 V, I_S = 100 A)

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Figure 10 shows a comparison of the probes under a more aggressive switching condition. In the comparison, two points of interest are highlighted. First, at turn-off, the Rogowski coil cannot adequately capture the shape of the current waveform, missing the slight knee which will decrease the apparent switching losses. Additionally, the reduced di/dt predicted at turn on will also contribute to a lower predicted switching loss. The cumulative effect of the Rogowski coils reduced bandwidth is a decreased estimate of switching losses.

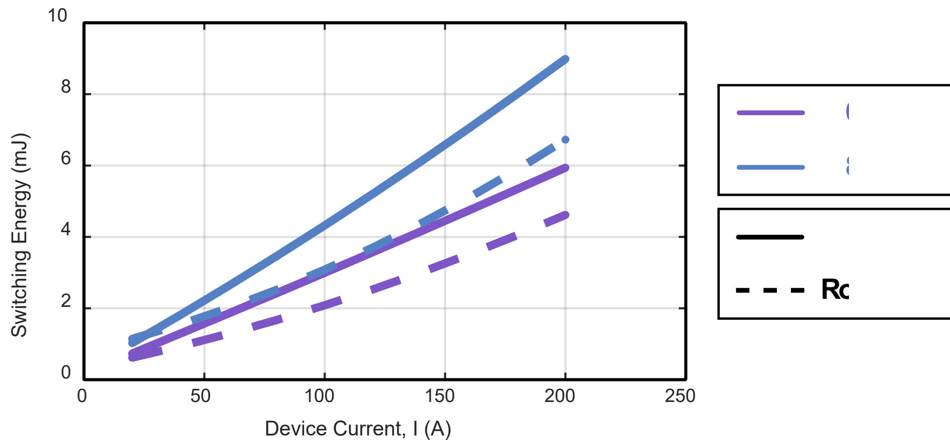

Figure 11. Switching loss ($E_{Off} + E_{On}$) estimation using different probes (CAB011M12FM3, $T_J = 150°C$, $R_G = 1\ \Omega$)

Figure 11 shows a direct comparison of the estimated switching losses for the CAB011M12FM3 across drain current. As mentioned above, the Rogowski coil consistently underpredicts the switching losses of the circuit, giving an overly optimistic impression of the circuit losses. Because the discrepancy is related to the probe bandwidth limitations, it is dependent on edge rates of the transistor, and will increase with more aggressive gate resistances. For slow switching technologies (such as IGBTs) the difference in metrology may be negligible.

2.5.2 Drain Voltage Measurement

Figure 12. Probe examples, (a) Tektronix differential probe THDP0200 (1500 V Range),
(b) Tektronix TPP0850 voltage probe

Two common methods for voltage measurement in power electronics systems are differential probe and the ground referenced probe. The differential probe is a popular choice since it can be added across arbitrary nodes of the circuit without issue. The ground referenced probe, however, requires caution in implementation as its shield pin is attached to the earth ground of the oscilloscope. Incorrect implementation of a ground reference

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measurement will generally lead to small ground currents on the probe reference which substantially reduce the accuracy of the measurement. In more serious cases (where the ground reference shield is connected to a power signal), large currents can flow through earth ground destroying the probe or oscilloscope. In the worst case, a failed connection from the instrument to earth ground can cause the outer metal casing of the oscilloscope to float to the bus potential and pose a serious threat to operator safety.

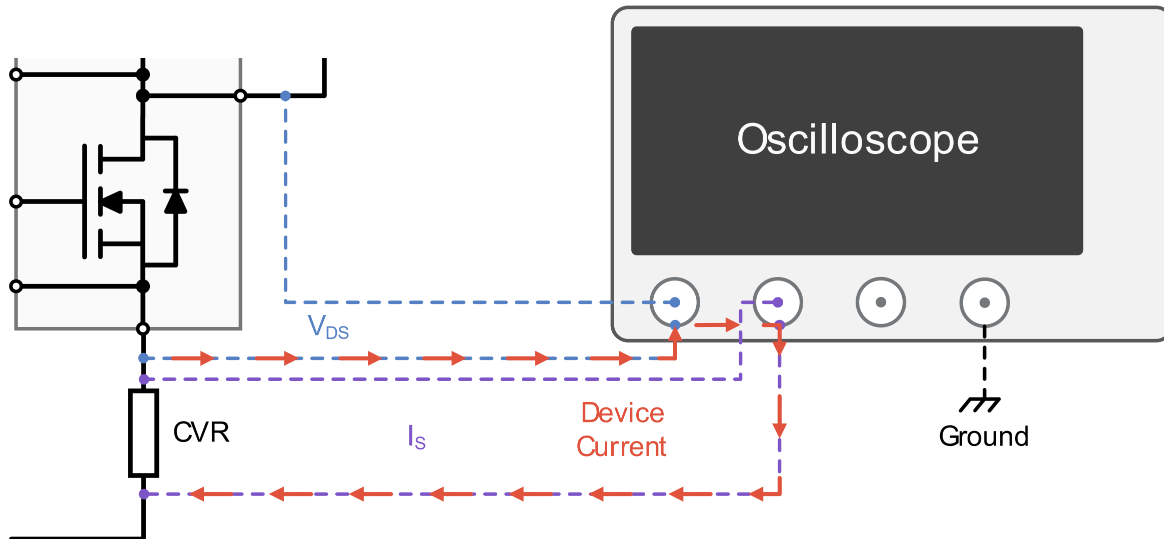

Figure 13. Potential grounding error when using CVR and ground reference probe

The grounding issue becomes more critical when also using a ground referenced CVR. As shown by Figure 13, when using a ground referenced probe in combination with a CVR, it is possible to bypass the CVR via the scope shielding path. This can lead to the entire device current flowing through the oscilloscope which is likely to destroy the voltage probe or oscilloscope. It also presents a substantial safety hazard. In general, differential probes are recommended for measurements of device drain to source.

2.5.3 High-Side Gate Measurements

Figure 14. Probe examples, (a) Tektronix differential probe THDP0200 (150 V Range), (b) Tektronix IsoVu TIVH05 (TIVPMX10X, ±25 V sensor tip)

Measuring the high-side gate of a power module comes with an additional challenge in that the source reference of the gate is connected to the midpoint of the module. Not only is this node not ground referenced,

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it also has very large changes in voltage during the switching events. This requires a measurement device which is both decoupled from ground and which features a very high common mode rejection ratio. The traditional metrology for this high-side gate voltage measurement is a standard differential probe, but newer, optically-isolated probes can make this measurement more accurately.

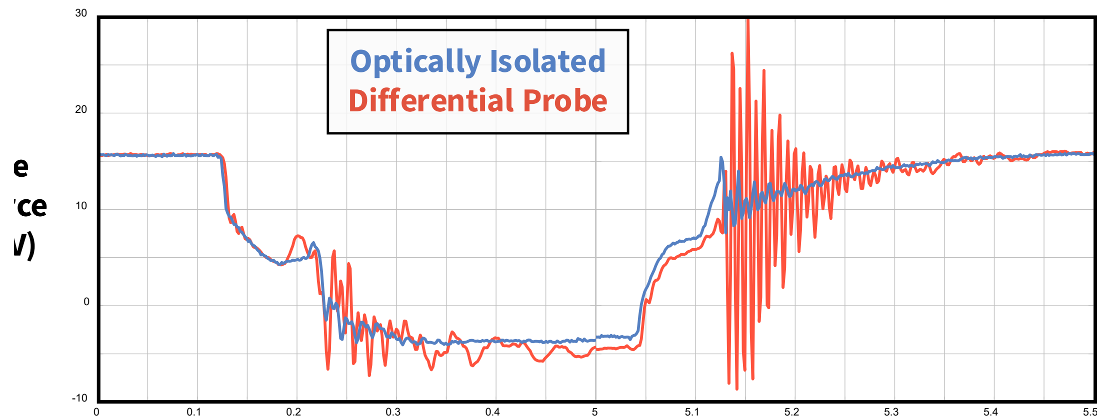

Figure 15. Differential probe vs optically isolated probe, CAB016M12FM3 (T_J = 150°C, V_{DS} = 800 V, I_S = 200 A)

Figure 15 shows a comparison of the high-side gate voltage for the standard differential probe versus the optically isolated probe. Both at turn-off and turn-on, high frequency ringing can be seen on the gate after the device's gate passes through the threshold region. Due to coupling between the gate and power loop, some ringing is expected. However, in the case of the differential probe, the ringing has a significantly higher amplitude than is measured by the optically isolated probe. This is likely due to the changing reference voltage inducing common mode currents within the probe and an artifact of the standard differential probe. While the waveform measured by the differential probe in Figure 15 appears to pass the maximum gate voltage of the device, the more accurate measurement of the optically isolated probe makes it clear that the device is within specification. Application designers using standard differential probes for gate voltage measurements should use caution as it may not be possible to differentiate between the measurement artifact shown here and an actual violation of the device ratings.

3. Design Guidance for Optimal Dynamic Performance

This section gives various recommendations for achieving optimal dynamic performance with the CAB011M12FM3. Module performance is influenced by external factors such as converter layout, gate drive design, and thermal management system. This section gives recommendations for electrical system design to help optimize module performance in application.

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3.1 Power Loop Layout Recommendations

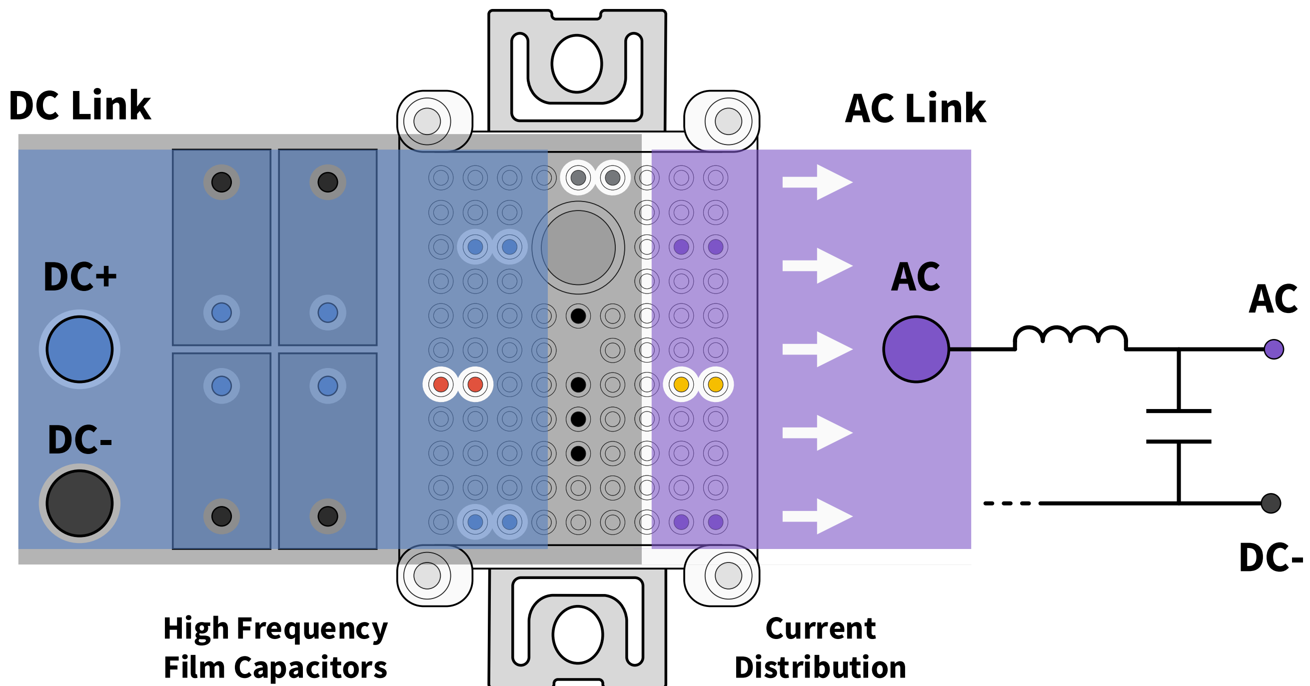

Figure 16. Recommended high-performance PCB layout

Layout of SiC MOSFETs in power electronics applications is not a trivial design task. Because of the high voltage, high current, and (relatively) high frequency, the layout poses several overlapping challenges which may conflict with each other.

A critical design goal of converter layout should be elimination of parasitic inductance in the DC link, as increase in this inductance leads to increase in voltage overshoot during switching transients. Figure 16 shows several strategies to minimize this inductance.

- First, in addition to bulk capacitance on the DC link, high frequency capacitors are placed in proximity to the module, functioning as decoupling capacitors. As these capacitors are intended to supply the energy during transient events, a rule of thumb for calculating capacitance is 10x the total module switching energy ($E_{ON}(Q1) + E_{OFF}(Q1) + E_{ON}(Q2) + E_{OFF}(Q2)$). Film capacitors are recommended for the high frequency capacitors as they are more robust than ceramic capacitors and have lower parasitic inductance than electrolytic capacitors.
- Next, copper planes are used rather than traces; these should be as large as possible given the available area and sized to meet the DC current specification. Additionally, multiple planes can be interleaved to maximize flux cancellation between layers, which will generally lead to a lower inductance than a single pair of thick copper planes. While magnetic coupling would preferably be maximized by thin substrates between layers, remember that the inter-layer thickness will be determined by the DC voltage divided by the material's dielectric strength. Consider including a margin of safety as large potential transients can induce partial discharges which slowly break down dielectrics over time.

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The layout of Figure 16 also avoids overlap between the AC output plane and the DC- plane. Coupling between these conductors will introduce additional parasitic output capacitance to the low-side MOSFET, which negatively impacts dynamic performance and increases switching losses. Because the AC terminal of the module is usually connected to a filter inductance, parasitic inductance in this connection is not a significant factor in module performance. The AC link should instead be sized for current capacity.

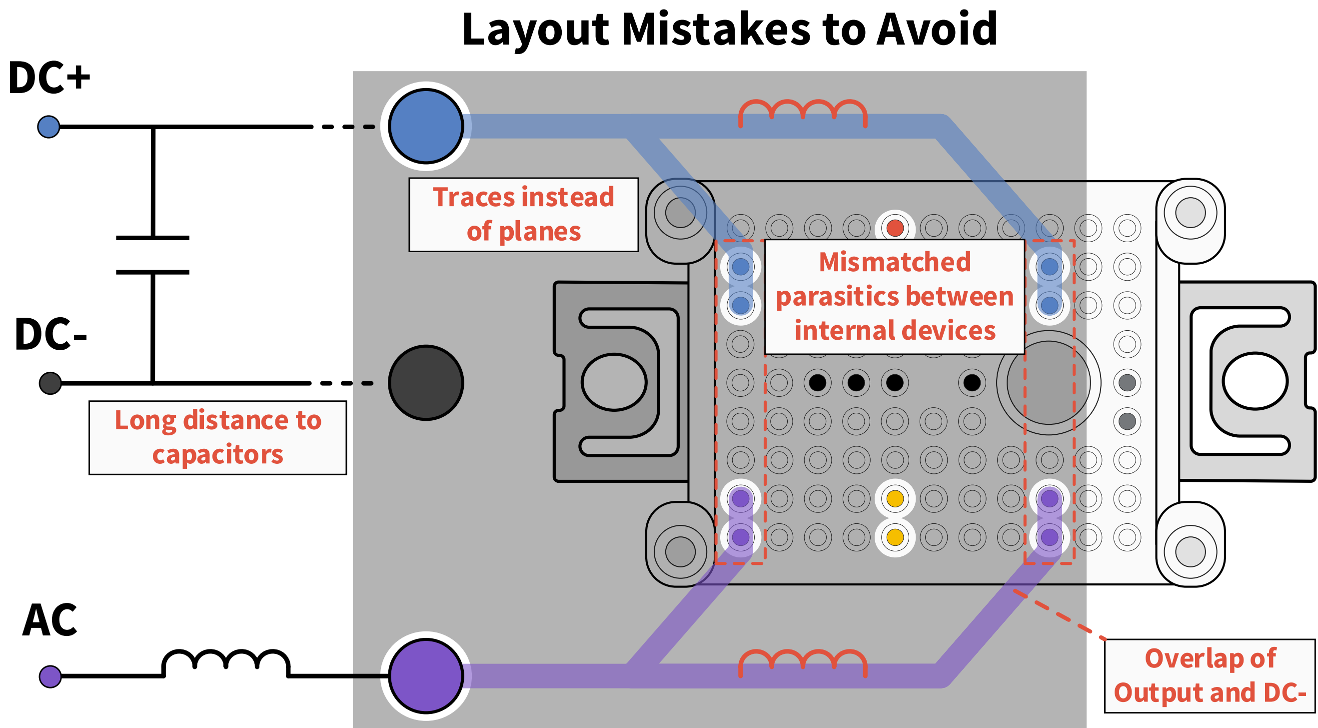

Figure 17. Layout mistakes to avoid

To better emphasize the design ideas integrated into Figure 16, an alternate layout with several design mistakes is shown in Figure 17. Rather than using a plane for DC+, traces are used, which increases the series inductance. This is further exacerbated by a significant electrical distance to the DC link capacitors. This high series inductance will lead to substantial overshoot at turn-off. Another mistake is the overlap between DC- and AC output, increasing parasitic capacitance across drain to source of the low-side MOSFET. Using a trace for DC-, however, would be a very poor solution to this issue, as this would significantly increase series inductance on the DC bus.

The final issue shown in Figure 17 is more subtle; the perpendicular layout of the module leads to unequal parasitic inductance between switch positions of the module. This imbalance will lead to a mismatch in dynamic current sharing between the parallel MOSFETs which can cause higher voltage overshoot and reduced device lifetime.

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3.2 Gate Loop Layout Recommendations

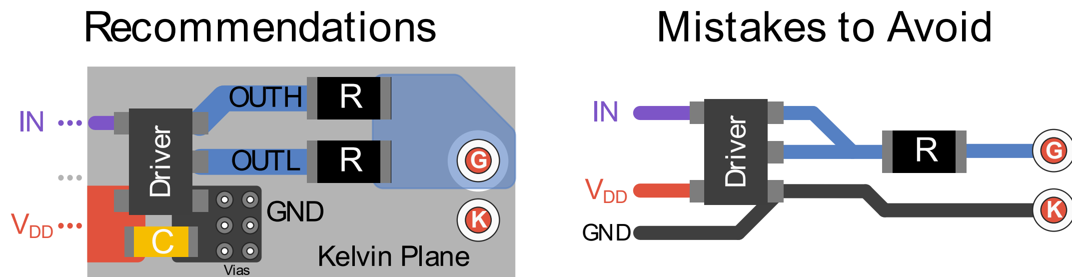

Figure 18. Recommended gate layout for unipolar architectures

Figure 18 shows general guidelines for layout of a unipolar gate driver (for example using a gate drive bias of +15 V / 0 V). To minimize gate loop inductance, a small plane for the kelvin connection should be placed on a layer adjacent to the gate connections. While this kelvin plane internally connects to the source of the MOSFET, it should not be connected externally to the power source. Linking these conductors will introduce common source inductance and reduce module performance. If the driver IC offers dual output channels, separate resistors for turn-on and turn-off are recommend (more information on Gate Resistor selection can be found in Section 3.4).

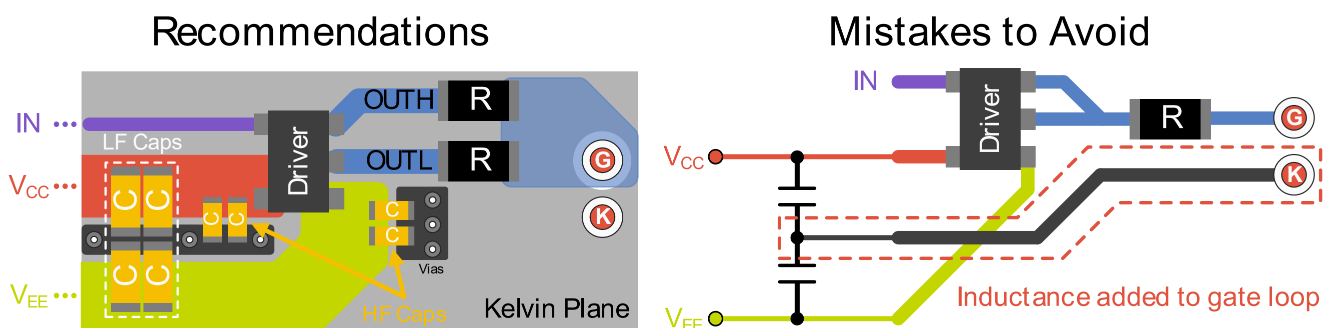

Figure 19. Recommended gate layout for bipolar architectures

Figure 19 shows general guidelines for gate driver layout when using split voltage rails (for example using a gate drive bias of +15 V / -4 V). General layout practices, such as use of power planes and decoupling capacitors, are recommended. Additionally, high frequency capacitors (such as 10 nF) are necessary to create a return path from the kelvin connection to the driver IC. Larger decoupling capacitors should also be implemented per the driver IC's datasheet recommendations.

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3.3 General Module Performance

Module switching losses are given for the CAB011M12FM3 over external gate resistance, junction temperature, and source current. Additional performance information can be found in the datasheet.

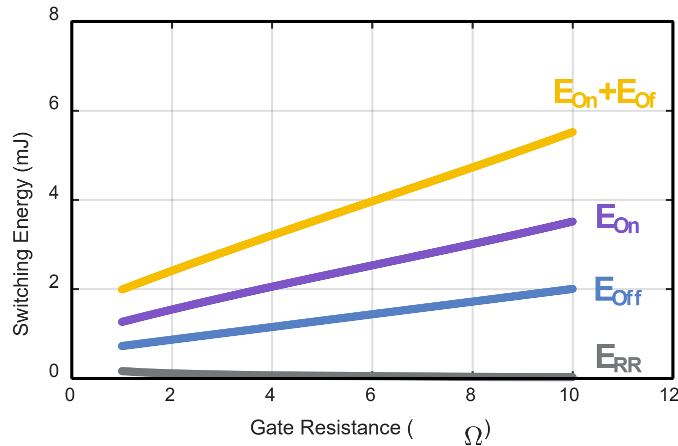

Figure 20. Switching losses versus gate resistor (T_J = 25 °C, V_{DS} = 600 V, I_S = 100 A)

The speed of the switching transient depends on the external gate resistance, a higher gate resistance will lead to increased switching losses.

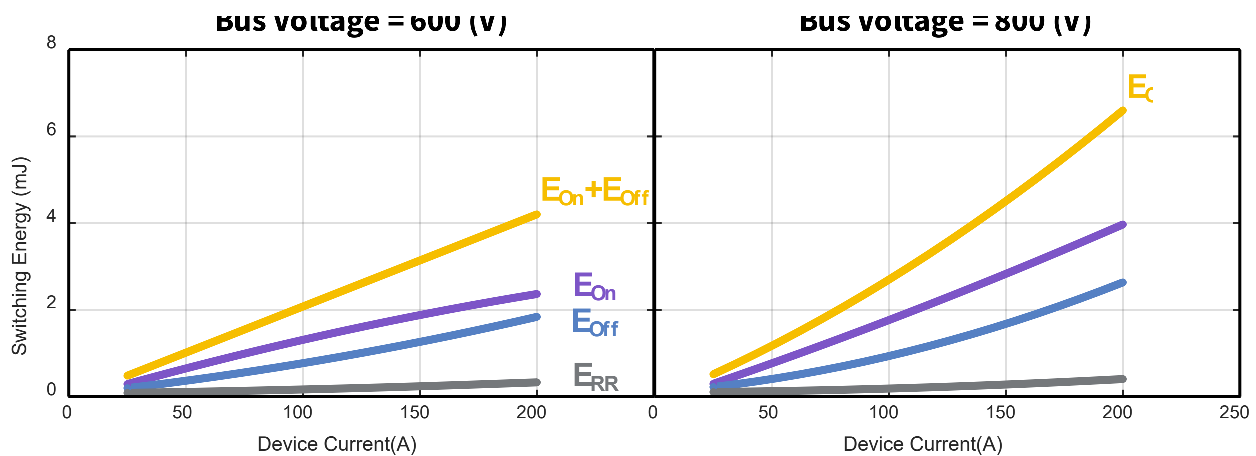

Figure 21. Switching losses versus current (R_G = 1 Ω, T_J = 25 °C)

The losses are also dependent on the current and voltage present during switching.

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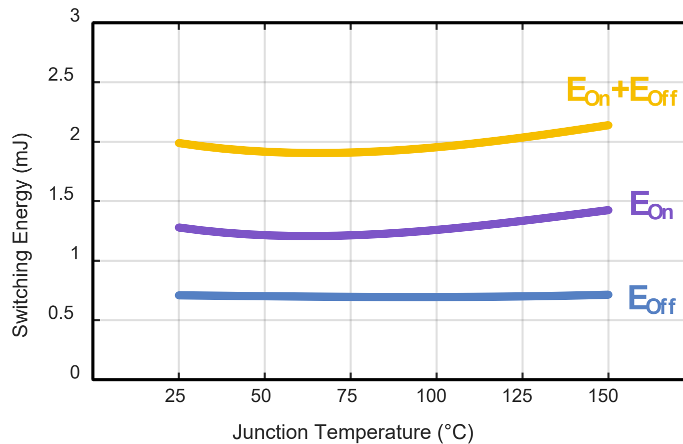
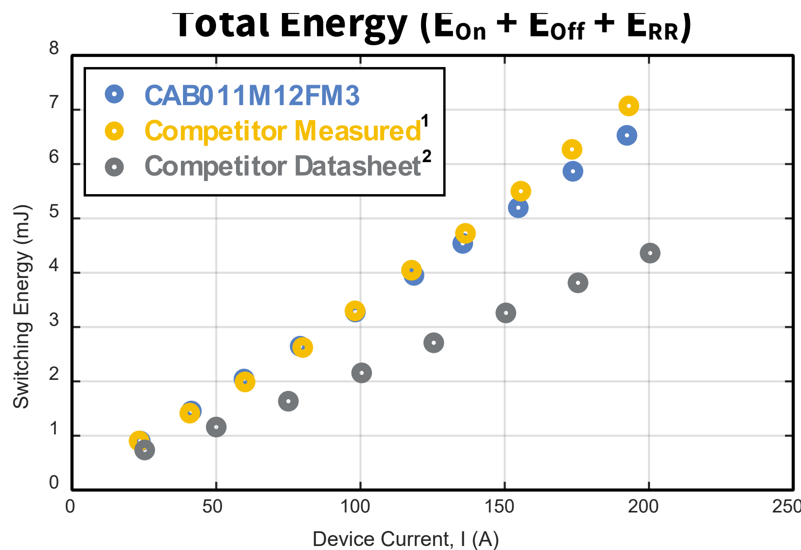


Figure 22. Switching losses versus junction temperature (V_{DS} = 600 V, I_S = 100 A, $R_{G\text{-}EXT}$ = 1 Ω)

Although less significant than gate resistance, switching losses are also dependent on device temperature.



[1]V_{GS} = -3 / +15V, R_G = 4.0 Ω, V_{DS} = 600 V, T_{VJ} = 150 °C
[2]V_{GS} = -5 / +15V, R_G = 3.9 Ω, V_{DS} = 600 V, T_{VJ} = 150 °C,

Figure 23. Comparison between CAB011M12FM3 and compatible competitor part (V_{DS} = 600 V, T_J = 150 °C)

In addition to evaluation of the FM3 modules, the DPT evaluation tool can be used with pin-for-pin compatible competitor parts. Figure 23 shows one comparison which provides results that could be expected testing the module with Wolfspeed hardware and partner gate drivers.

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3.4 Selection of Gate Resistor

While lower gate resistance is preferred for reduced switching losses, selection of external gate resistor is a critical design tradeoff between device reliability and performance. A specification for maximum tolerable overshoot should be determined and used to set a minimum allowable external gate resistance.

NOTE: The following guidelines and overshoot values are for only applicable to the **CAB011M12FM3**, and not to other module variants in the FM3 family. Additionally, the overshoot values given are contingent on a properly designed PCB interface and local decoupling capacitors. Consider designing a margin of safety into fielded applications.

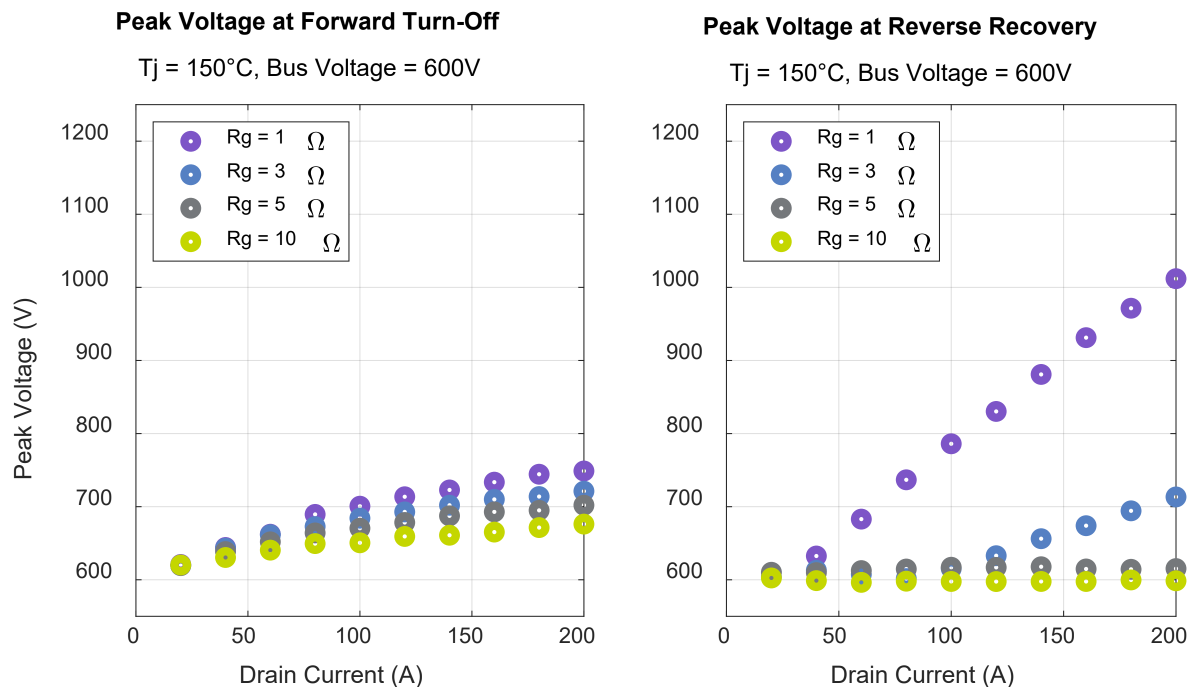

Figure 24. Peak voltage versus gate resistance, (V_{DS} = 600 V, T_J = 150 °C)

Figure 24 shows the peak voltage overshoot measured during transient events versus gate resistance and device current for a 600 V bus. The results were measured using the CIL evaluation kit described in Section 2.2. These overshoot values will increase with higher parasitic inductance, so the layout recommendations of Figure 16 should be followed to minimize inductance. These values for device overshoot are measured outside the power module and are modestly lower than the actual voltage overshoot seen by the device (due to internal inductance in the module).

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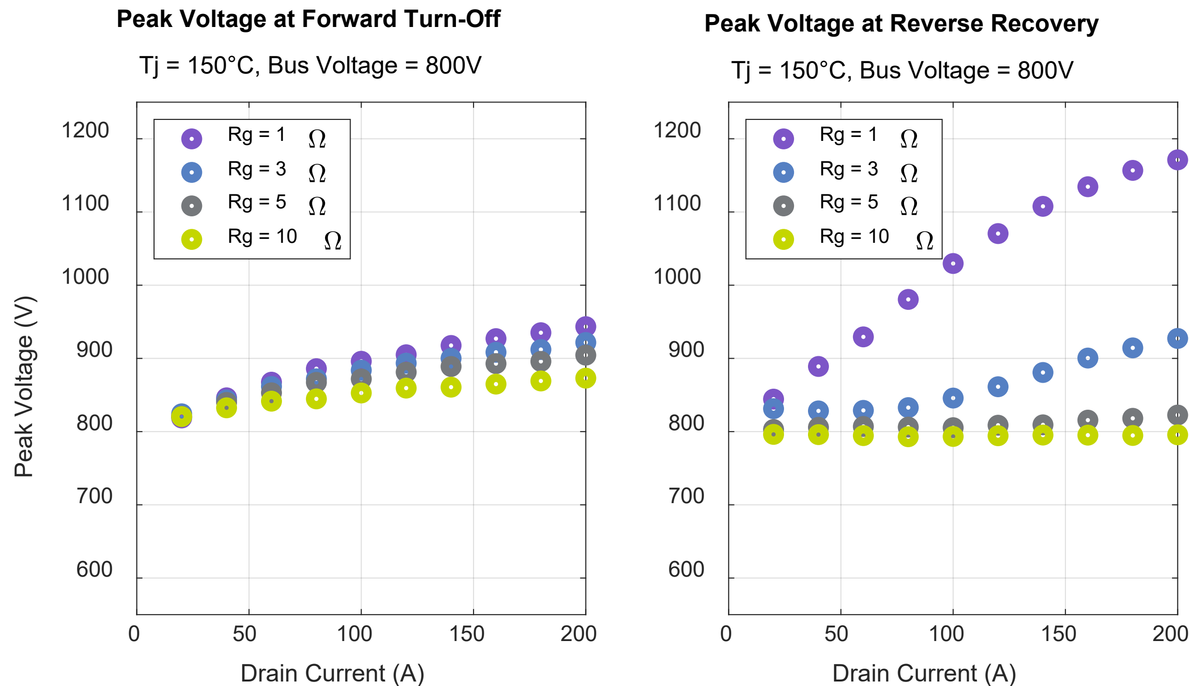

Figure 25. Peak voltage versus gate resistance, (V_{DS}=800 V, T_J = 150 °C)

Figure 25 shows the voltage overshoot when evaluated with an 800 V bus. With higher bus voltages, the margin for transient overshoots is reduced. It is important to note that lower stray inductance designs are possible, especially for a final system without the CVR. It is recommended that the module's overshoot is evaluated in the final system to ensure that voltage overshoot margin is maintained or improved.

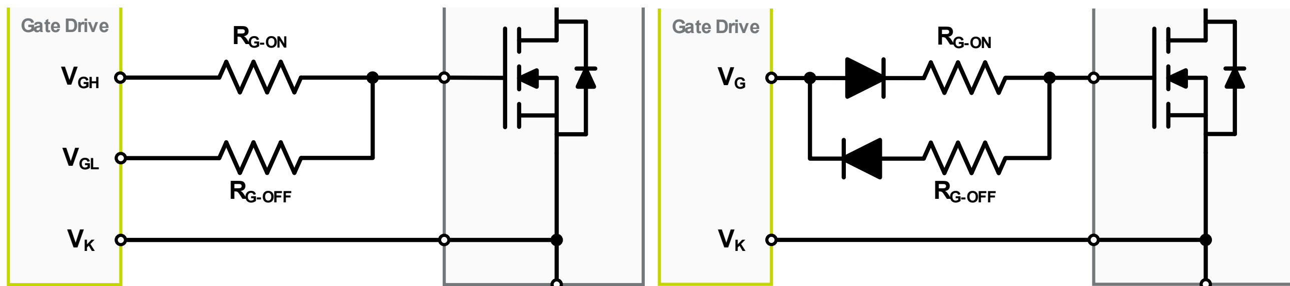

Figure 26. Separate selection of R_{G-ON} and R_{G-OFF}

As shown in Figure 19, many gate drive IC's have separate drive pins for gating the transistor on and off. Even when using a simpler, single-output gate drive, Figure 26 shows how diodes can be used to separate the external gate resistor into both on and off values. In addition to distributing the R_G power requirements across two resistors, selecting separate on and off resistors can be used to better optimize the tradeoff between switching loss and voltage overshoot. R_{G-OFF} will control the overshoot and losses at turn-off while R_{G-ON} will control the overshoot and losses at turn-on.

An important caveat is that reverse recovery losses are determined by R_{G-ON} of the actively gate switch, not the gate resistance of the MOSFET whose body diode is conducting the current. Using the typical low-side DPT as an example (shown in Figure 4), the reverse recovery losses in Q1 occur when Q2 turns on. The amount of

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recovery losses will be determined by the slew rate (di/dt) of the current. This slew rate is determined by the speed Q2 turns on (which has nothing to do with the gate resistance of Q1). Therefore, the recover losses of the high-side switch should be considered in the selection of $R_{G\text{-}ON}$ for the low-side switch.

3.5 Gate Driving Options

As mentioned in the Section 3.2 (Gate Loop Layout Recommendations), gate driving can be conducted with unipolar (ex: +15 V / 0 V) or bipolar (ex: +15 V / -4 V) voltage rails. While the using bipolar topologies increases gate drive complexity and cost, it leads to a reduction in dynamic losses. Additionally, negatively biasing the gate of the MOSFET in the off state improves resilience to EMI by providing additional headroom before threshold is reached. Thus, oscillations on the gate pin are less likely to trigger the MOSFET and potentially cause shoot through events.

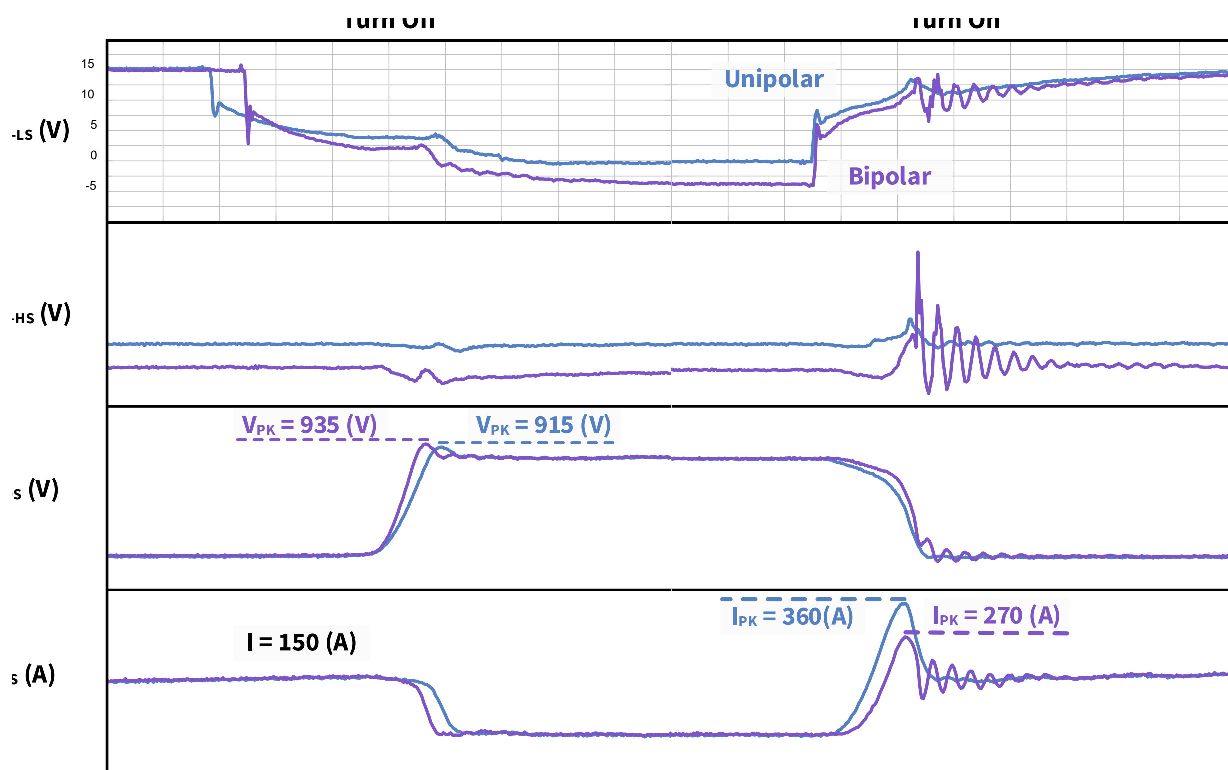

Figure 27. Unipolar vs Bipolar, time domain comparison (T_J = 150°C, V_{DS} = 800 V, I_S = 150 A, $R_{G\text{-}EXT}$ = 4 Ω)

Figure 27 shows a comparison of the time domain waveforms of the module when driven with unipolar and bipolar topologies. While the faster switching of bipolar at turn off leads to a marginal increase in voltage overshoot, this can be compensated for by increasing $R_{G\text{-}OFF}$, as described in Section 3.4.

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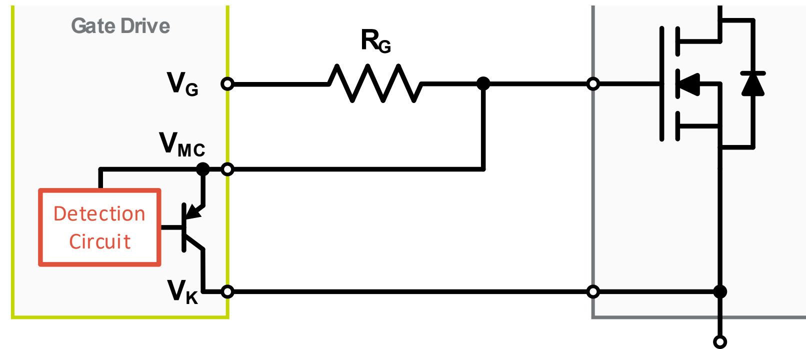

Figure 28. Miller Clamping Circuit

Another important consideration in gate drive design is miller clamping. This is often a feature built into gate drive ICs and is used to prevent the device from turning-on due to voltage induced on the gate from currents through the miller capacitance (C_{DG}). As Figure 28 shows, this function is accomplished by monitoring the voltage on the MOSFET gate and "clamping" it with a transistor when the detection circuit is activated.

Miller clamping is especially important when using a unipolar gate drive or a low negative gate drive rail. This is because the gate bias when the part is off is close to threshold and relatively small induced voltages will cause false triggering (and generally current shoot through). Figure 29 through Figure 31 show time domain comparisons of these driving techniques for the CAB011M12FM3 at 1, 5, and 10 Ω. Figure 29 shows turn on, Figure 30 shows turn-off, and Figure 31 shows reverse recovery.

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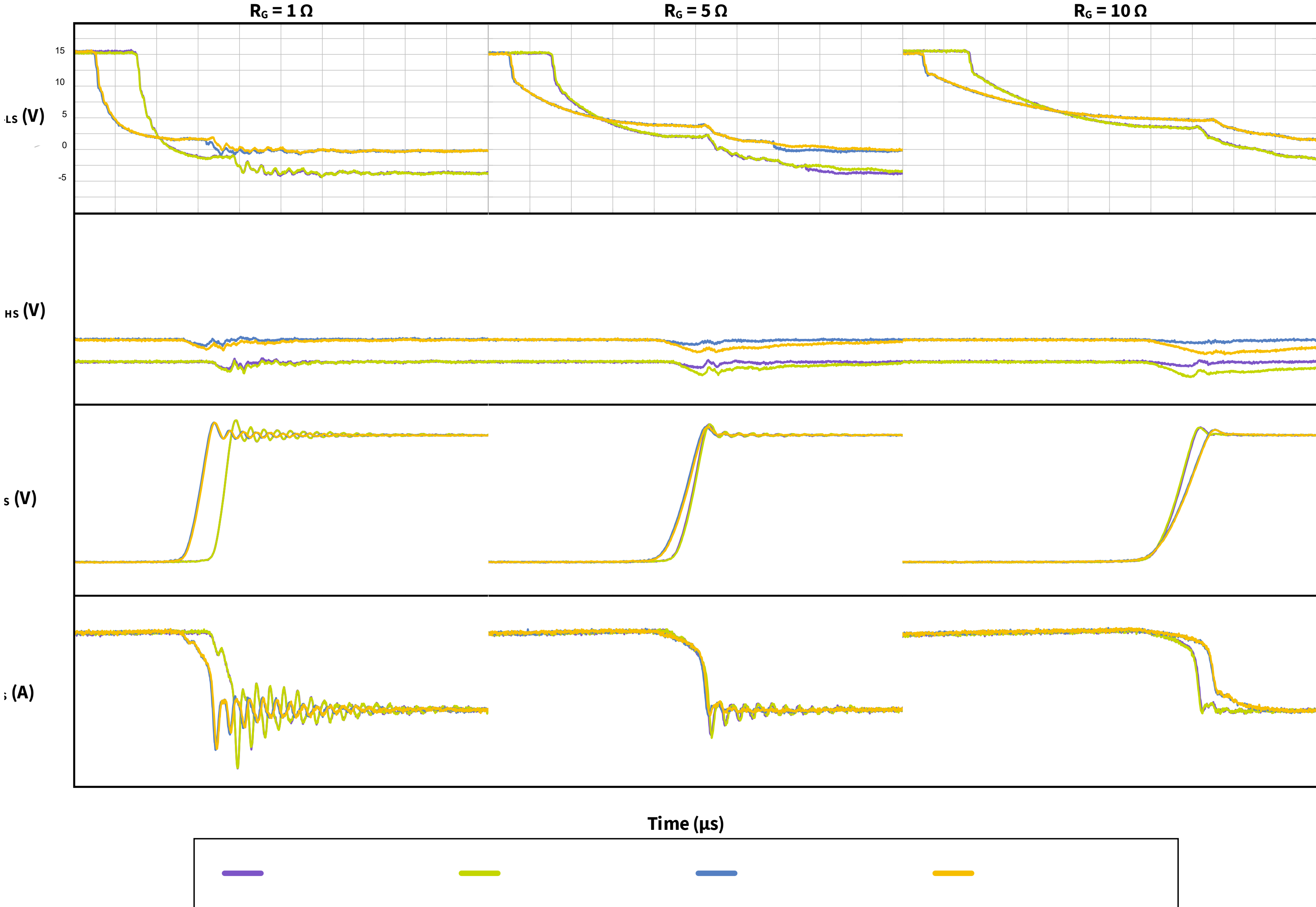

Figure 29. Waveform comparison, reverse recovery (T_J = 150°C, V_{DS} = 800 V, I_S = 100 A)

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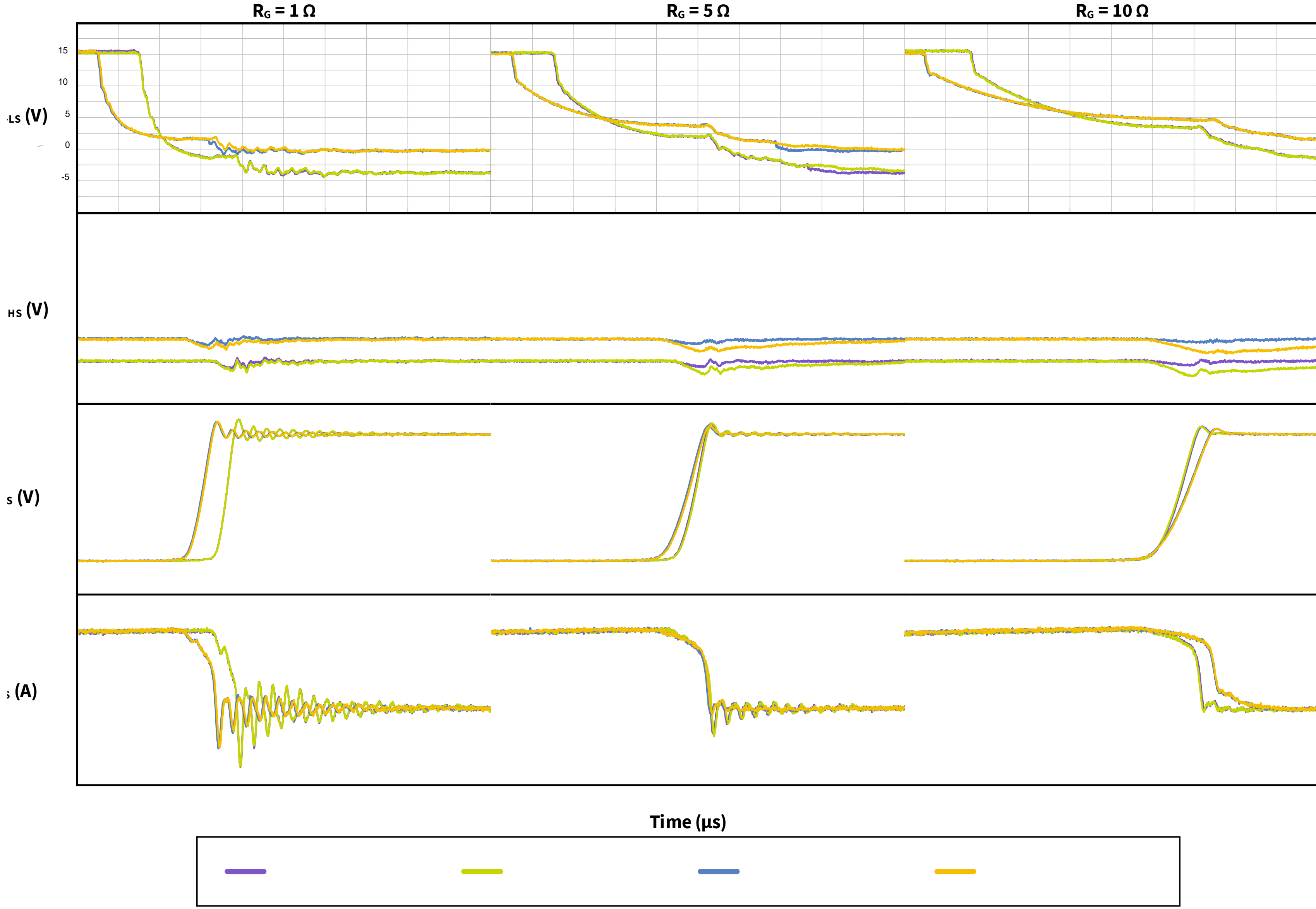

Figure 30. Waveform comparison, reverse recovery (T_J = 150°C, V_{DS} = 800 V, I_S = 100 A)

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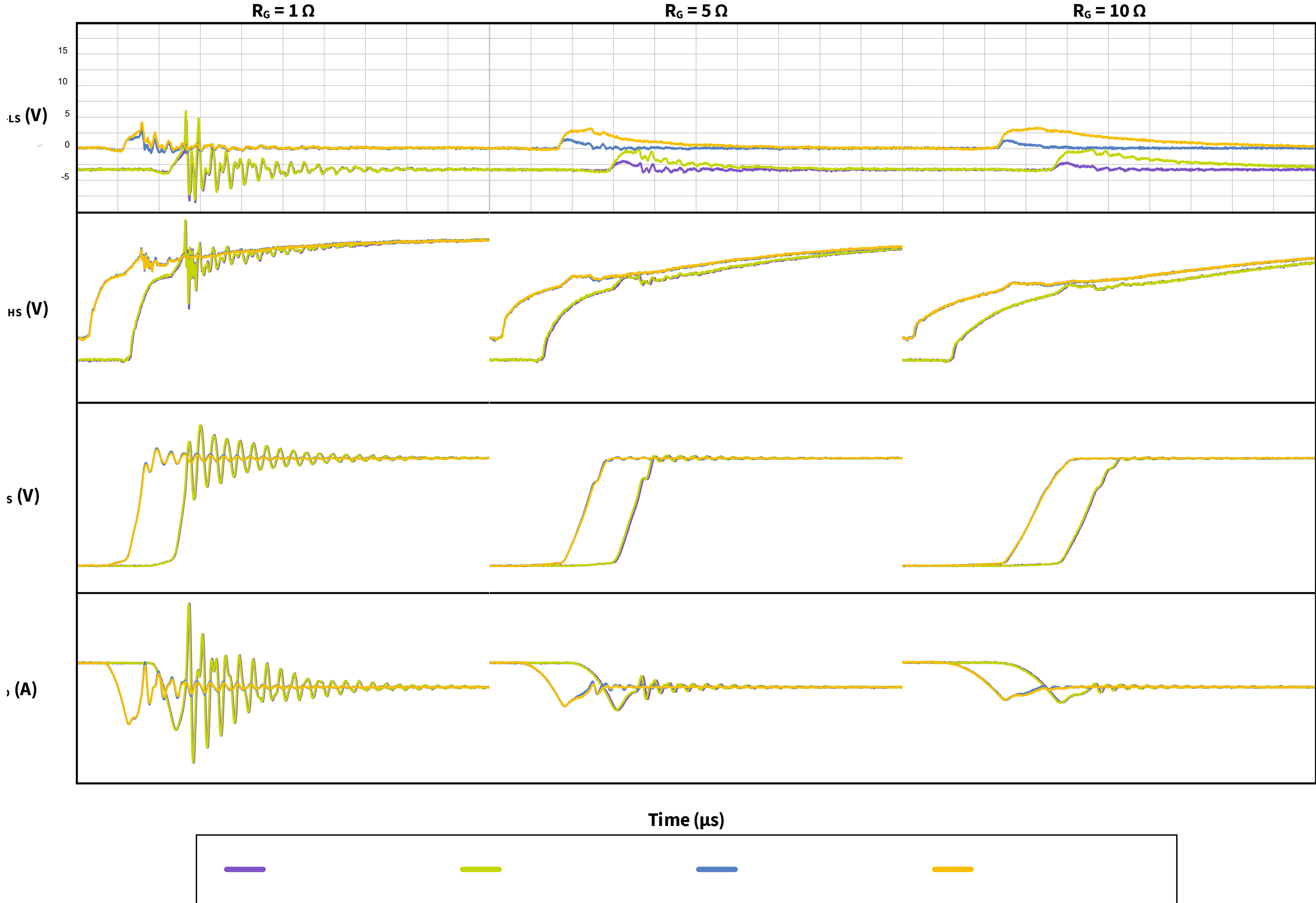

Figure 31. Waveform comparison, reverse recovery (T_J = 150°C, V_{DS} = 800 V, I_S = 100 A)

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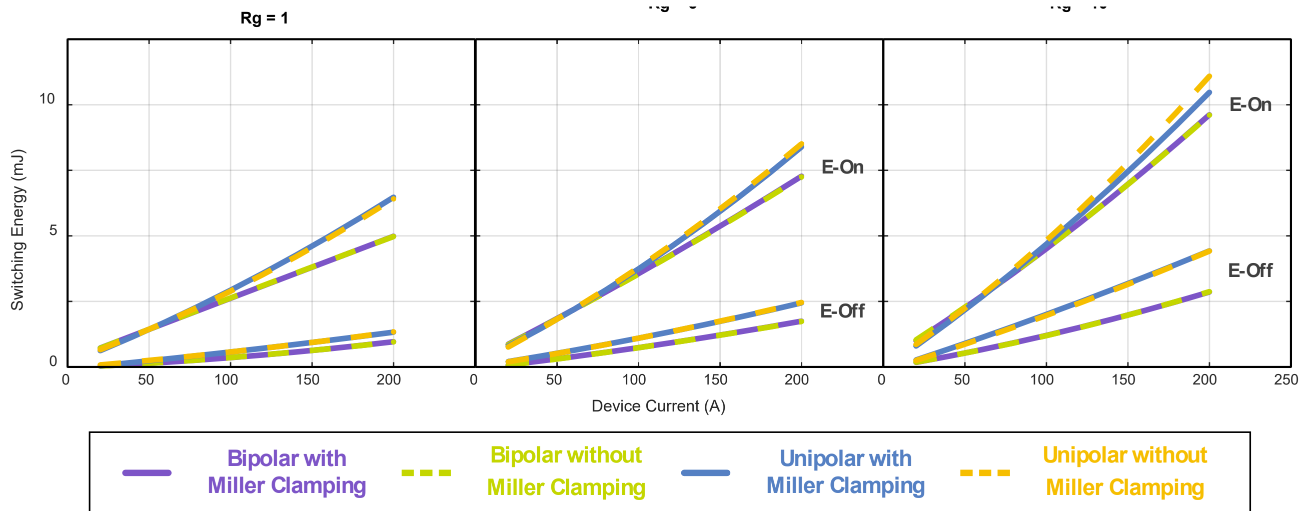

Figure 32. Loss comparison, Unipolar vs Bipolar, with and without Miller Clamping (T_J = 150°C, V_{DS} = 600 V)

Figure 32 gives an overview of the loss comparison between unipolar and bipolar driving schemes at 600 V. It also shows the influence of miller clamping. This highlights the reduction in switching losses when using bipolar driving, and shows that miller clamping does not substantially influence the system losses.

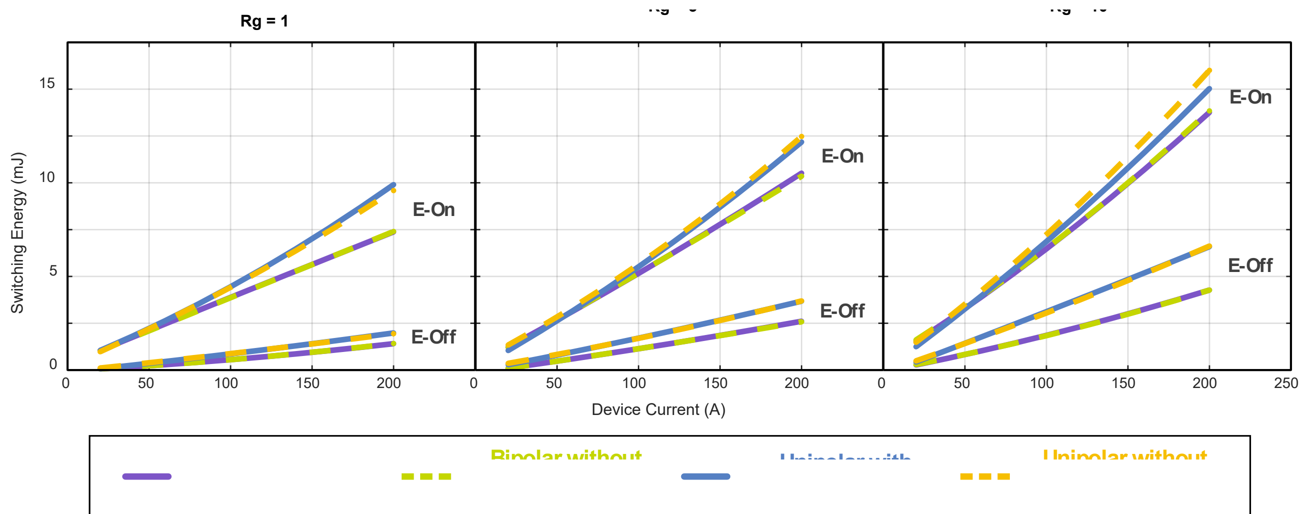

Figure 33. Loss comparison, Unipolar vs Bipolar, with and without Miller Clamping (T_J = 150°C, V_{DS} = 800 V)

Figure 33 shows that while losses increase at 800 V, there is not a significant change to the trends originally identified at 600 V.

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Revision History

Date	Revision	Changes
January 2021	1	Initial Release
January 2024	2	Formatting Updates

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