Simulation of power amplifiers (PAs) for modern wireless base station and small cell systems is an essential part of the design process. At a cell site, the PA consumes the bulk of the DC power, generates the most heat, and thus represents the greatest operational cost. Maximum PA efficiency is a necessity to manage these costs, which is a sizeable challenge in a PA that also must be highly linear to support the complex multi-level modulation types and wide bandwidths used for current and developing wireless transmission standards. Accurate simulation allows the PA designer to meet these challenges by exploring the available design options, then optimizing the circuit that is selected for the application.

High performance power devices such as GaN HEMTs are combined with sophisticated circuit architectures to achieve the necessary efficiency and linearity. The PA may use any of several different design methods — Doherty, envelope tracking, outphasing, or any of several extensions and hybrid structures — but in each case it must be optimized for the highest efficiency while maintaining all other desired performance characteristics.

PA design and optimization requires accurate and complete simulation tools, including sophisticated models of power device behavior. To this end, Cree, Inc. has developed 6 port large signal model capability that is being added to all models for its GaN HEMT devices [1]. The ports include:

- Gate
- Source
- Drain
- Temperature
- Intrinsic drain voltage
- Intrinsic drain current

![Figure 1. Large-signal model schematic in Microwave Office™.](image_url)
The models are compatible with both Agilent's ADS and AWR's Microwave Office design suites. The complete model in Microwave Office™ is shown in Figure 1. The core large-signal model is based on established equivalent circuit methods, with data extracted in various test fixtures and test circuits, including load pull at the fundamental and harmonics.

The intrinsic drain current and intrinsic drain voltage ports are newly-developed additions to the device model. Intrinsic means that these virtual ports are located right at the active device, without the effects of package parasitics. To the designer, these intrinsic ports act as voltage and current probes right at the die. This ability to observe the voltage and current waveforms is essential to verify the PA's class of operation and to optimize device matching at fundamental and harmonic frequencies.

In addition, observing drain voltage is important for investigation of drain voltage switching, peak voltage excursions or drain modulation, as is used in multi-level Doherty and envelope-tracking PAs. Also, circuit robustness can be evaluated by observing peak voltages during high VSWR conditions.

Unlike traditional classes A, B and C that are defined by device bias conditions and sine wave signals, high efficiency classes of operation (classes E, F, and others) utilize the active device as a switch. Performance is defined by the relationship between current and voltage, including the shape of the waveforms, which is a function of the energy at harmonic frequencies. The PA designer must develop input and output bias and matching networks that fulfill the requirements for the desired class of operation. Optimized design, where practical implementation approaches ideal behavior, can only be accomplished when the PA engineer can observe the actual drain voltage and current waveforms in addition to the traditional parameters of input power, output power, DC power and bias.

Readers are certainly aware that digital predistortion (DPD) is a critical part of achieving the necessary linearity for accurate signal modulation and minimum off-channel energy that can interfere with other users. They should note that DPD is intended to be the final step in the linearization process. It is most effective when the uncorrected path through the amplifier chain has the highest performance obtainable.

**Class F and Inverse Class F Operation**

Presently, class F and inverse class F are favored for high efficiency designs. For ideal class F operation, the drain voltage waveform is a square wave and the current waveform is a half-sine (Figure 2) [2]. Ideal inverse class F operation, as the name implies, has a square wave current waveform and a half-sine voltage waveform (Figure 3) [3]. Ideal square waves contain an infinite number of harmonics which is not possible in a practical PA. However, a small number of odd harmonics (e.g., 3rd and 5th harmonic) will result in a sufficient approximation of a square wave to obtain high power added efficiency (PAE). Figures 4 and 5 show practical waveforms for class F and inverse class F PAs.
Figure 2. Ideal class F waveforms.

Figure 3. Ideal inverse class F waveforms.

Figure 4. Practical class F waveforms.
Figure 5. Practical inverse class F waveforms.

To obtain a practical waveform that approximates the ideal shape, an accurate simulation model is required. It is not practical to physically probe the drain voltage and current at the die, and probe points located at the edge of the package will be altered by impedance transformation through the package leads. Even with bare die mounting, bond wires add series inductance and parasitic capacitance. In any case, a physical probe will have its own parasitic effects on the circuit.

From the above discussion, we see that waveform engineering enables the design of high efficiency switch-mode power amplifiers. These classes of amplification are defined by (and their performance requires) specific waveforms for voltage and current at the device drain. In the time domain, we want to assure that the waveform shape is an acceptable approximation of the ideal condition. In the frequency domain, we want to control the amplitude of the odd harmonics (typically 3rd and 5th) necessary to achieve approximately square waveforms, while cancelling the unwanted even harmonics.

Figure 6 illustrates why intrinsic drain voltage and current ports are important. Fig. 6(a) shows the voltage and current waveforms at the edge of the transistor package. Note that current goes negative, which will occur when there is reactance between the drain and the measurement point. The reactance also results in a phase shift between the package plane and the device drain, as the current and voltage waveforms do not have the necessary anti-phase relationship. The intrinsic port waveforms are shown in Fig. 6(b). With the correct observation point, the phase alignment of voltage and current are now correct, and the current has only a slight negative excursion. The dynamic load line I-V curves of Fig. 6(c) (in red) are undistorted by the package inductance and parasitic capacitance. Drain current is positive, and the shape of the curves shows the intended result of waveform engineering—close to zero current at high drain voltages, with maximum current at low drain voltages.
Figure 6. Comparison of waveforms at intrinsic ports and package plane. (a) shows the waveforms at the extrinsic reference plane that includes package effects; (b) shows the waveforms at the intrinsic port located at the device; and (c) shows the dynamic load line curve family.
Finally, the desired waveform must be achieved using the impedance transformation networks at input and output. Synthesis, optimization and realization of a matching network that operates over the desired bandwidth is the traditional work of an RF PA engineer, and has become increasingly difficult with the additional requirements of proper harmonic response for the PA class of operation and the wider bandwidth required for high data rate wireless communications systems.

2 GHz Class F Design Example

To demonstrate the design process, we present a class F design centered at 2 GHz [4]. The device selected is a Cree CGH60015D GaN HEMT. First, a series of source- and load-pull simulations were performed using the AWR Load Pull Wizard, which simulates bench measurements. The sequence of these virtual measurements was:

- Source-pull for gain at fundamental frequency
- Source-pull for power at fundamental
- Source-pull for PAE at fundamental
- Load-pull for gain at fundamental
- Load-pull for power at fundamental
- Load-pull for PAE at fundamental
- 2nd harmonic load-pull for PAE
- 3rd harmonic load-pull for PAE

The above sequence illustrates how device input and output impedances were optimized at the fundamental frequency for best PAE after maximizing gain and output power. PAE of 72% was obtained when both source and load were matched. Next, the effects of the load network impedances for the 2nd and 3rd harmonics were analyzed. After some iteration to correct for the effect of harmonic loads on the fundamental, the optimized termination of the harmonics resulted in a PAE of >80%.

Using the input and output impedances determined by the above source- and load-pull simulations, matching networks were synthesized that corresponded closely with the required gate and drain impedances at the fundamental and harmonics. The input network is shown in Figure 7. The transformed impedances presented at the Gan HEMT gate are shown in Figure 8.
**Figure 7.** Input matching network for the 2 GHz class F PA example circuit.

**Figure 8.** Impedances presented to the gate of the active device.

The PA output matching network is shown in Figure 9, with the corresponding impedances seen by the drain shown in Figure 10.
Figure 9. The example PA output matching network, which transforms the fundamental and appropriately terminates the 2nd and 3rd harmonics.

Figure 10. Fundamental and harmonic impedances presented at the GaN HEMT drain.

Figure 11 shows the full schematic of the class F PA using the CGH60015D device. Note the $\lambda/4$ shunt transmission line in the drain bias supply. This line presents a high impedance for odd harmonics and a low impedance for even harmonics. Even harmonics are effectively shorted, as required for class F operation. The output signal path has a series tuned resonator that passes the fundamental and reflects the odd harmonics back to the drain, where they contribute to the drain voltage waveform.
Figure 11. The complete schematic of the example class F PA.

Figure 12 is a plot of gain, power output and PAE versus input drive power. At maximum output power the PAE reaches a peak value of 84%. Figure 13 shows PAE at full output versus frequency. This plot illustrates that class F is relatively narrowband in this implementation. However, techniques are available for significantly wider bandwidth, as required for the newest wireless standards.

Figure 12. 2 GHz gain, PAE, DC to RF efficiency and power output versus drive power.
Constructing the PA After Simulation

The example circuit was developed through extensive simulation effort. Implementing this design in practice required some refinements in the input and output matching networks, as shown in Figures 14 and 15. For the input network, stabilization resistors were added at the cost of a small reduction in gain. The output network provides harmonic termination in the bias line and impedance matching in the RF output line.

Figure 14. Modified input network for a practical 10 watt class F PA.
Figure 15. Modified output network for the practical implementation.

Measured performance data for the constructed PA is shown in Figure 16, and Figure 17 is a photo of the completed amplifier. This circuit may be used stand-alone for small cell base station, or it may be used as a building block in a combined high-power PA, a multi-level Doherty PA, or any other architecture that will benefit from an efficient PA element.

Figure 16. Performance plots of the constructed PA.
Summary

Advanced simulation tools, supported with complete and accurate device models, are a necessary part of power amplifier design for wireless communications (and other applications in the GHz frequency range). High efficiency and predictable performance over a range of drain voltages and backoff points are achieved using high performance power devices such as GaN HEMTs.

Repeatable performance is needed to support multi-amplifier architectures that are used in many PA systems. Again, accurate models increase the designer’s confidence in classic statistical analysis with real-world component variations and fabrication dimensional tolerances.

Contact Information

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References