RELIABILITY OF GaN/AlGaN HEMT MMIC TECHNOLOGY ON 100-mm 4H-SiC

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Abstract

This paper reports the reliability performance of the Cree, Inc., GaN/AlGaN HEMT MMIC process technology, fabricated on 100 mm high purity semi-insulating (HPSI) 4H-SiC substrates. The Cree V3 process technology is based on a 0.4 µm gate length GaN HEMT designed for 28 V applications and includes metal-insulator-metal (MIM) capacitors, NiCr thin film resistors, and low-resistance source vias that are small enough to embed inside the transistor technology.

I. Introduction

Cree currently manufactures and sells a complete line of commercial GaN discrete transistors for both general purpose (military, civil, industrial, and scientific) and wireless (4G, LTE, WiMAX) applications. The general purpose discrete parts currently support a number of military production systems including military communications, counter improvised explosive device (C-IED) systems, radar, and a variety of other industrial applications. Cree also develops and produces high-power GaN MMIC products to support a variety of commercial and defense applications, including a 2 W, 20 MHz - 6.0 GHz MMIC driver amplifier and a 25 W, 2.5 - 6 GHz MMIC power amplifier. These products are currently in production and have been successfully fielded in a variety of harsh application environments.

II. Process Technology

Cree's GaN HEMT MMIC process technology for 28 V applications, referred to as G28V3, has been fully qualified for volume manufacturing. Cree has shipped devices amounting to a grand total of approximately 1.3 MW of RF power from the G28V3 process. The salient features of the process technology include:

- Semi-insulating 4H-SiC wafers 4 mil thick 3" or 100 mm in diameter
- GaN epitaxial layer stack grown by metal-organic chemical vapor deposition, consisting of AlN nucleation layer, Fe-doped GaN insulating buffer, AlN barrier, and undoped $Al_{0.22}Ga_{0.78}N$ active layer, resulting in a sheet resistance R_{SH} of 340 Ω/□
- Gates 0.4 µm long with extension for built-in electric field plate
- Source-connected second field plate
- 100 V metal-insulator-metal (MIM) capacitors (180 pF/mm^2)
- NiCr evaporated thin film resistors (12 Ω/□, 10 µW/µm^2, 1 mA/µm)
- Bulk resistors (70 Ω/□ and 400 Ω/□)
- Two Au metal levels 3 µm thick with dielectric crossovers
- Solderable back-side with Au metallization
- Slot-shaped, low resistance through-wafer vias 30 x 75 µm, embedded directly in the HEMT devices
- > 150 V breakdown
- > 4.5 W/mm & 65% PAE @ 28 V operation (3.5 GHz)
- DC-8 GHz performance

III. 28 V Qualification

The G28V3 process technology fabricated on 3" wafers was qualified for volume manufacturing using a comprehensive set of acceptance tests on packaged discrete HEMT devices with 3.6 mm gate periphery. The devices were assembled using the production process for Cree's released product CGH40010, which features a 1:1:1 CuMoCu cavity-style package with AuSn eutectic die attach. Three process lots were sampled at 77 devices per lot. The following qualification acceptance tests were all passed with zero device failures out of 231 devices per test, which demonstrates a least tolerable percent defect (LTPD) level of 1, with 90% statistical confidence:

- 28 V DC high temperature operating life at 4 W/mm, 85 °C case temperature, and 225 °C junction temperature, for 1000 hours (MIL STD 883G Method 1005)
- High temperature reverse bias at 84 V drain voltage, -8 V gate voltage, at 150 °C ambient temperature for 1000 hours (MIL STD 883G Method 1005)
- Temperature cycling -55 °C to +150 °C for 1000 cycles (JESD22-A104, Condition H, Soak mode 1)

- High temperature storage life 200 °C ambient temperature for 72 hours (JESD22-A103)

Subsequently, the process technology was converted to 100 mm SiC wafers. The same device construction was employed to qualify the 100 mm wafer process technology. The G28V3 process technology on 100 mm wafers was successfully qualified in a similar manner as on 3" wafers, using a total of 472 devices.

The following additional suite of stress tests was employed to characterize the process technology to environmental conditions, electrical over-stress, and electro-static discharge:

- Electro-static discharge human body model (ESD-HBM), 5 pulses per terminal (JESD22-114)
- Electro-static discharge charged device model (ESD-CDM), 5 pulses per terminal (JESD22-C101)
- Temperature-humidity bias (THB), 28 V drain voltage, -8 V gate voltage, 85 °C, 85% relative humidity for 500 hours

The results demonstrated an ESD-HBM classification of 1A (> 250 V), an ESD-CDM classification of class III (> 500 V), and passing results from THB.

Temperature cycling on via chain test structures showed no significant change in via resistance after 200 cycles from -55 °C to + 150 °C. This demonstrates the good mechanical reliability performance of the embedded through-wafer vias.

Constant-current stress on NiCr thin film resistor test structures shows negligible change in resistance after 1000 hours at 175 °C and 2.8 mA/mm (which is 2.8X the rated current of 1 mA/mm).

These reliability results on the discrete passive elements further support the robustness of the HEMT MMIC process for the targeted application conditions.

IV. Channel Temperature Estimation

For normal operation, qualification, and reliability tests, the channel temperature is estimated as the maximum junction temperature in the channel just under the gate corner on the drain side. Infrared (IR) microscopy and finite element analysis (FEA) are employed to produce accurate channel to case temperature differentials, from which a θjc (peak junction to case thermal resistance) is calculated. An iterative process is employed, in which an IR image is taken for a given power dissipation and base plate temperature. The FEA is the spatially averaged and compared with the IR image. The thermal resistance is a modeled parameter that is adjusted iteratively until agreement is achieved between the IR and FEA. The resulting thermal resistance is then used to estimate the maximum junction temperature for a given power dissipation and case temperature.

V. 28 V Intrinsic Reliability

The 28 V intrinsic reliability performance of the HEMTs was assessed using DC accelerated life tests (ALT) on discrete 3.6 mm HEMT devices with source vias. The ALT was performed at 28 V DC stress, 6 W/mm, and up to 380 °C maximum junction temperature, as calculated using the method described above. Approximately 15 devices per ALT stress temperature were sampled from 3 wafer lots. Devices were periodically removed from the ALT system and run through Cree's production DC and RF device test suite, which consists of a variety of tests including on resistance, pinch-off, 84 V breakdown, IDSS, small signal gain, and saturated power and efficiency. Individual device failure criterion is determined by either catastrophic fail or by 1 dB decrease in saturated power, compared to its initial value.

Fig. 1 shows the ALT results on devices from 3" wafers. The Arrhenius fit yields an activation energy of 1.8 eV. A wider range of stress temperatures could not be achieved due to constraints on both ends: At higher temperatures, a secondary failure mode is introduced that is over-accelerated and not a concern for recommended operating conditions. Lower temperatures result in lifetimes that exceed many months duration. The intrinsic lifetime is predicted to exceed 10^7 hours at 225 °C and 10^9 hours at 175 °C. The extrapolation was substantiated by a test that was launched at 325 °C; although median lifetime was not reached after 1500 hours, extrapolation of the saturated power degradation predicted a median lifetime of ~28,000 hours, which is in good agreement with the extrapolated curve.

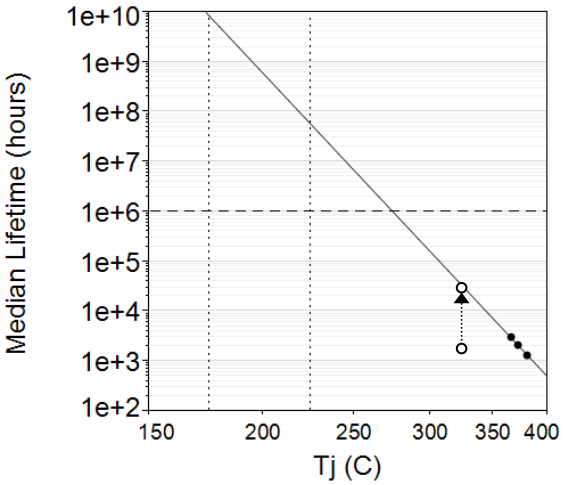

Fig. 1. Median lifetime versus junction temperature for 28 V DC ALT at 6 W/mm on devices fabricated on 3" SiC wafers. Solid symbols represent median lifetimes of 10-15 devices per stress temperature. Open symbols represent a suspended test with lifetime extrapolated to 1 dB saturated power degradation. Solid line is Arrhenius fit to solid symbols and extrapolation to operating conditions.

Fig. 2 shows the ALT results on devices from 3" and 100 mm wafers. The median lifetimes from both process technologies are comparable, and so the data is treated as equivalent and analyzed as a whole. The Arrhenius fit yields an activation energy of 1.6 eV, which is not statistically different from the result obtained on devices from 3" wafers only. The intrinsic lifetime is predicted to exceed $5*10^6$ hours at 225 °C and $3*10^8$ hours at 175 °C. The result demonstrates excellent and comparable intrinsic reliability performance for devices on 3" and 100 mm wafers.

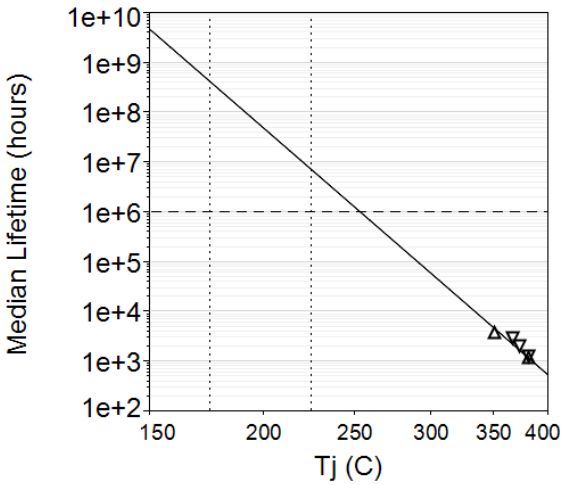

Fig. 2. Median lifetime versus junction temperature for 28 V DC ALT at 6 W/mm on devices fabricated on 100 mm (triangles) and 3" (inverted triangles) SiC wafers. Solid line is Arrhenius fit to all data and extrapolation to operating conditions.

Fig. 3 shows the lifetime distribution at 380 °C ALT conditions for devices from 100 mm wafers. The results give a lognormal sigma value of 0.33.

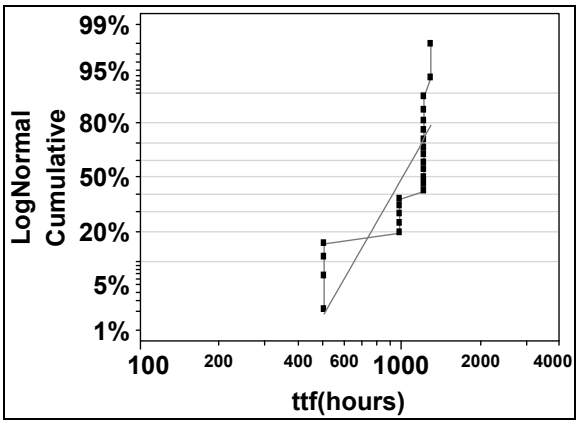

Fig. 3. Lognormal lifetime distribution for 24 devices fabricated on 100 mm wafers at ALT conditions at 380 °C junction temperature.

Fig. 4 shows SEM and TEM images of a device after ALT stress at 380 °C that has degraded more than 1 dB in saturated power. The images show intermetallic mixing of the ohmic contacts and gold interconnect metal only on the source side, not on the drain side. This is also evident from top-down inspection showing discolored source metal. In addition to the saturated power degradation, the on resistance also increases throughout the ALT. However, no evidence has been observed of inverse piezo-electric lattice deformation after 28 V ALT, as

has been reported elsewhere. In addition, no evidence has been observed of gate sinking. These observations are typical of several devices that have undergone physical failure analysis after saturated power degradation resulting from ALT stress. These results are consistent with source metal intermixing being the primary degradation mechanism in ALT and therefore also at normal operating conditions. The results are also consistent with AlGaN cracking not being a relevant failure mechanism for Cree devices under 28 V operation.

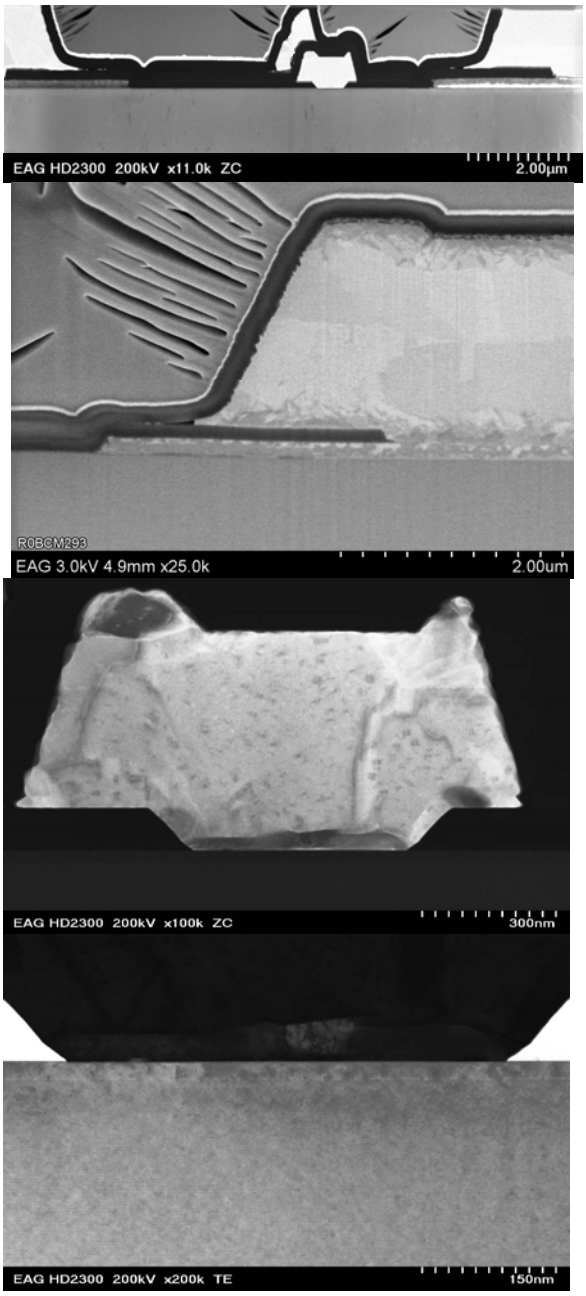

Fig. 4. Electron microscope images of a HEMT device after ALT stress that induced 1 dB degradation in saturated power.

The DC ALT results are substantiated by the RF ALT result shown in Fig. 5. The result shows that the output power degrades approximately 1 dB after 800 hours, which is consistent with the measured lifetimes in the DC ALT tests shown in Fig. 1. In addition, the result on this large periphery device shows that the result is independent of device size, which is encouraging that the intrinsic reliability performance is equivalent for all sizes of Cree devices in production.

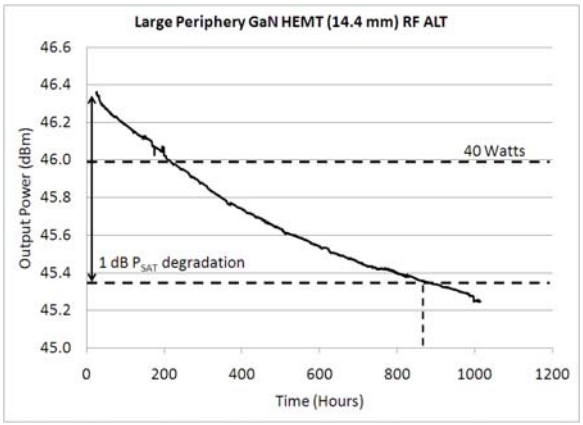

Fig. 5. Output power versus time for a large periphery (14.4 mm) GaN HEMT device under RF ALT stress conditions of 28 V, Idq = 1.0 A, input power 37 dBm, dissipated power 3.3 W/mm, case temperature of 200 °C and junction temperature of 380 °C.

The reliability performance of MIM capacitors was assessed using ramped voltage breakdown measurements. Results from ”intrinsic” small area capacitors showed a field acceleration coefficient of 2.8 cm / MV and activation energy of 0.15 eV. \ Fig. 6 shows the results of ramped voltage breakdown testing of “extrinsic” large area (0.1 mm) MIM capacitors. The results show that approximately 95% of extrinsic capacitors are predicted to have a lifetime of over 10^6 hours at 100 V and 85 °C. This result therefore predicts reliable operation for RF applications at 28 V with comfortable margin.

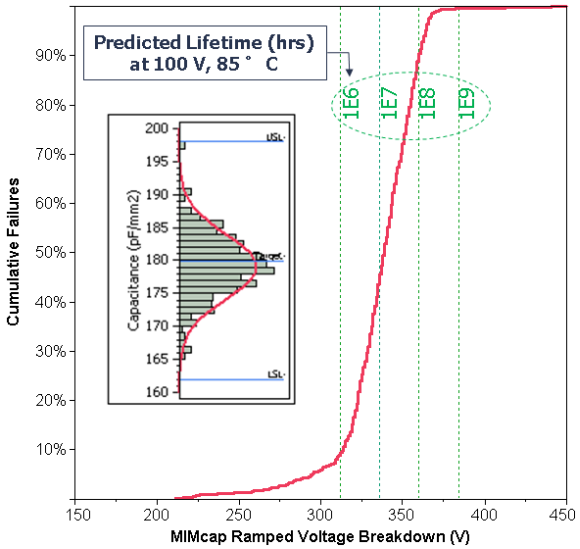

Fig. 6. MIM capacitor ramped voltage breakdown distribution. Dashed lines show predicted lifetime at 100 V and 85 °C. Inset shows distribution of capacitance and specification limits.

VI. Reliability Data from the Field

The excellent intrinsic reliability performance predictions are supported by field returns data. Cree’s GaN parts have been shipping since Jan 2007 and have logged 1.4 billion hours in the field (assuming that the devices are on half of the time). Conservative estimates on the number of valid field failures result in a FIT rate of 8.6 fails / billion device hours. This FIT rate predicts a median lifetime of 6800 years, with 60% statistical confidence, which is consistent with the ALT intrinsic lifetime predictions. This FIT rate indicates that Cree’s GaN HEMT devices appear to already be on par with, or better than, other established RF technologies.

VII. Conclusion

In conclusion, intrinsic reliability testing on discrete HEMT devices, MIM capacitors, and thin film resistors, demonstrates excellent intrinsic reliability performance of the Cree V3 GaN/AlGaN HEMT MMIC process technology on 3” and 100 mm SiC substrates, for 28 V RF applications up to 6 W/mm.