Thermal Analysis and its application to High Power GaN HEMT Amplifiers

A. Prejs, S. Wood, R. Pengelly, W. Pribble

Cree Inc., Durham, NC 27703 USA

Abstract **– A systematic and consistent approach to the thermal modeling and measurement of GaN on SiC HEMT power transistors is described. Since the power density of such multilayered wide bandgap structures and assemblies can be very high compared with other transistor technologies, the application of such an approach to the prediction of operating channel temperatures (and hence product lifetime) is important. Both CW and transient (i.e. pulsed and digitally modulated) thermal resistances are calculated for a range of transistor structures and sizes as a function of power density, pulse length and duty factor and compared with measured channel temperatures and RF parameters. The resulting thermal resistance values have then been imported into new "self-heating" large signal models so that transistor channel temperatures and the resulting effects on RF performance such as gain, output power and efficiency can be determined during the amplifier design phase. Some practical examples are included in the paper including the temperature rises in the carrier and peaking transistors of a high power Doherty amplifier.**

Index Terms **– GaN, SiC, thermal simulation, IR scan, large-signal model, thermal resistance, transistor amplifier.**

I. INTRODUCTION

As with all semiconductor devices, SiC MESFET and GaN HEMT device reliabilities are dependent directly on maximum operating channel temperature. It is therefore important to determine, with a high degree of confidence, what the maximum channel temperature is under specific operating modes, particularly for products operating under CW conditions and dissipating large amounts of thermal energy. In addition to understanding the maximum channel temperature of a device for reliability, it is equally as important to understand thermal resistance of packaged transistors for system level design.

II. THERMAL RESISTANCE DETERMINATION

A dual-mannered approach is used in determining the thermal resistance of wide bandgap transistor & MMIC products. The use of Infrared (IR) microscopy and finite element analysis (FEA) are employed to produce accurate channel to case temperature differentials, from which a θ_{jc} (junction to case thermal resistance) can be calculated.

IR microscopy is performed using a Quantum Focus Instruments Infrascope II IR microscope at 5x magnification. A device under test (DUT) is placed into a suitable quarter inch thick test fixture for IR measurement. The test fixture is placed on top of a temperature-controlled heat sink. In order to gain visible access to the die surface, all DUTs must have their lids or plastic encapsulant removed prior to IR imaging. Dependent on the package type, the DUT is either bolted down or soldered into the fixture. For devices that are bolted down, a thin layer of thermal grease is applied to the bottom of the package to ensure that the least amount of contact resistance exists between the package and the fixture. Thermal grease is also used at the interface between the fixture and the heat sink. The fixtures used for IR imaging are modified such that a thermocouple can be placed under the backside of the package to monitor the package case temperature. All IR imaging is performed with the heat sink temperature set to 75°C for optimum device calibration. The package case temperature is then allowed to "float" and is monitored by the thermo-couple. A minimum of eight to ten devices from multiple lots are IR scanned to produce a significant amount of data points, which can then be correlated to FEA models. The devices are measured under DC drive at varying heat densities from 1W/mm to 8W/mm. Finite element analysis is performed using Ansys® software. The models are created in such a fashion that they reproduce how the devices are actually measured with the IR camera system. For all transistor applications this includes a packaged device in the fixture with the bottom of the fixture having a boundary condition of 75°C. If possible, models are sectioned as permitted by symmetry to reduce computational resources. See Fig. 1 & 2 for typical cross sections of a geometric model.

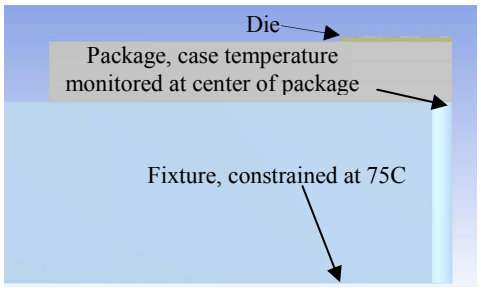

Fig. 1. Cross section of ¼ model.

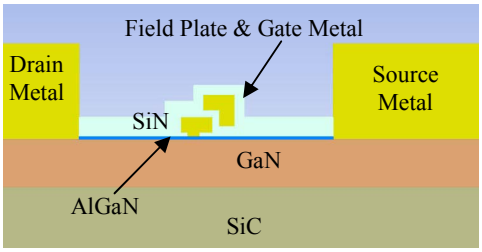

Fig 2. Cross section of gate area for a GaN HEMT showing SiC, GaN, AlGaN, Gate & Drain/Source Metals, Field Plate & SiN

Steady state thermal FEA is done using thermal conductivity (k) values as shown in Table 1. Temperature dependence is accounted for with GaN, SiC, & Au materials. Both the SiC & GaN are very temperature dependent and their k drops significantly with increase in temperature. GaN has a k of 130 W/mK at room temperature but at 300C it's k is reduced to 68 W/mK.

Material	Thermal Conductivity (W/mK)
GaN	130
AlGaN	19
SiN (passivation)	33
SiC	430
Au	317
AuSn (die attach)	57
CuMoCu (package)	300
Cu (fixture)	370

Table 1. Table of steady state materials properties.

To provide heat flux to the model a 0.4um heat source is used at the interface of the GaN / AlGaN layer and extruded to the appropriate length.

Once the IR camera and modeling data have been acquired, the thermal resistance of the device is calculated as:

$$\theta_{jc} = \frac{T_j\,(channel\ temperature) - T_c\,(case\ temperature)}{Dissipated\ Power} \quad (1)$$

It is important to note that the case temperature of the package (as measured by the thermocouple), and NOT the fixture is used for the calculations. The thermal resistance values represent only the packaged device.

Correlation of IR measurements to simulation results is done using a statistical analysis approach. It is important to note that the measured results produced by the IR imaging equipment are spatially averaged in areas of high heat flux. This is due to the resolution of the IR camera at 5x magnification being approximately 7 um while the actual heat source being less than 1 um in width and buried under various metal and passivation layers. The averaging effect produces measured data that is significantly lower than the actual peak channel temperature. To determine if the FEA data and IR data correlate, the averaged temperature of the FEA model is calculated across a 7um section centered on the heat source. A two-sided 95% confidence interval of the mean temperature rise is determined based on the IR measurement data. If the averaged FEA data falls within the confidence interval limits of the IR data, correlation between the model and IR data is considered successful. The peak temperature of the FEA model is used to establish the thermal resistance of the device. Figs. 3 & 4 show an example of how correlation is achieved for a 100um thick 14.4mm gate width GaN HEMT device mounted in a 60 mil thick copper-moly-copper package dissipating 4W/mm (58W) CW. The thermal gradient is very high surrounding the heat source and a thermal drop of about 58C is seen laterally at a distance of 3.5 um from the heat source in each direction. A 38C drop is seen vertically up through the AlGaN, SiN & metal layers along with a 46C drop through the 1.5um GaN layer. Although large thermal gradients exist in the x-y plane of the device and contribute to averaging effects during IR imaging, they do not exist in the z-direction due to large channel length to width ratios. The simulated thermal drop from channel to case is 157C, equating to a 2.72 C/W thermal resistance. The averaged thermal drop from channel to case is 113C, equating to 1.96C/W thermal resistance. This resistance falls within the confidence intervals of 1.89 C/W & 1.99 C/W as established by the IR data and shown in fig 4. Equivalent correlation has also been established at different power densities and devices types.

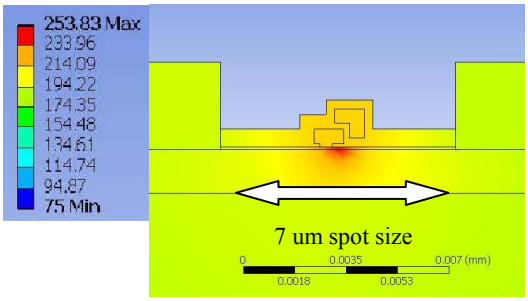

Fig. 3. Thermal profile near channel showing averaging effect across a 7um spot size.

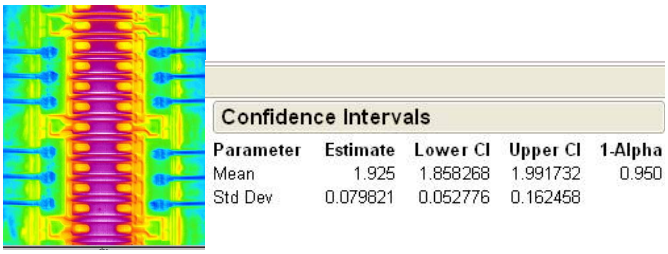

Fig. 4. IR measurement image & data for 14.4mm gate width GaN HEMT in 60mil thick CMC package.

III. SYSTEM IMPACT ON THERMAL RESISTANCE

In its simplest terms, the thermal resistance of a packaged device can be represented as the sum of a series of component resistances as shown below:

$$\theta_{jc} = \theta_{die} + \theta_{die\ attach} + \theta_{package} \quad (2)$$

Although this is a basic foundation, it is very important to understand that the total resistance is composed of many complex heat transfer mechanisms. Derived thermal resistance values are done under specific operating conditions. Using these values in a "casual way" to try and determine thermal resistances in scenarios other than how they were measured will lead to erroneous results. Simply changing the

power density in a 14.4mm gate width GaN HEMT device significantly affects the thermal resistance. An increase of 22% in thermal resistance is seen by increasing power density from 1W/mm (14.4W) to 4W/mm (57.6W). The increasing thermal resistance is driven by non-linearity of material properties as described previously. Similar types of unintuitive changes can occur when component thickness, package or fixture materials are made. Decreasing package thickness, for the same GaN HEMT device, from 60 to 40 mils together with a change in package material from CMC to CuW (K = 180W/mK) results in an overall thermal resistance increase of 16%. Upon examination, 10.5% of the thermal resistance increase is in the package. The remaining 5.5% increase is seen in the die. The decrease in thermal conductivity of the package explains the increase in package resistance. The increase in die resistance is due to lack of heat spreading within the die, which causes a larger thermal drop through the die.

IV. TRANSIENT ANALYSIS

Since many systems employing power amplifiers operate in modes other than CW, it is equally important to understand the transient response of a device. With almost an infinite number of pulse width and duty cycle combinations, an effective way of communicating θ_{jc} vs. time is essential. The best approach is plotting θ_{jc} vs. time in a semi-log scale for several duty cycles. In order to perform transient thermal analysis, density and specific heat material properties must be used in addition to thermal conductivity for time constant calculations of each material. The density and specific heat values used are listed in Table 2.

Material	Density (gm/cm^3)	Specific Heat (J/KgC)
GaN	6.1	490
SiC	3.1	681
Au	19.32	126
AuSn	14.5	150
Cu	8.3	385
Mo	10.3	250

Table 2. Materials Properties for Transient Analysis

Fig. 5 below shows the transient thermal response of a 28.8mm gate width GaN HEMT device in a 60mil thick CMC package dissipating 8W/mm of power at 10%, 20% & 50% duty cycles. The transient response shows two distinct slopes of resistance vs. time prior to full thermal saturation at approximately 400 milli-seconds. These two slopes can be attributed to the significantly different transient thermal properties of the die and package. Fig 6. shows how performing a transient thermal analysis with the same die but mounted into a 40 mil thick CuW package has the same thermal response during the first 100 mirco-seconds, but is significantly different after this point. The thermal resistance rise of the device with the CuW package is larger after 100 micro-seconds and can be explained by the slower thermal response of the CuW package.

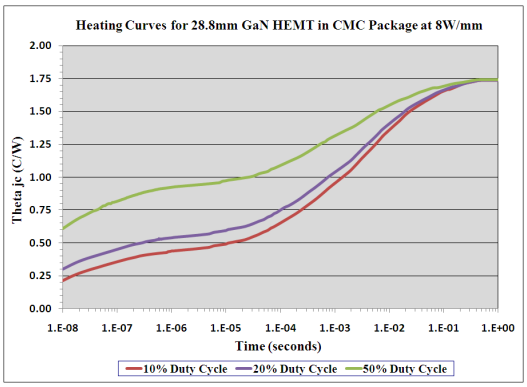

Fig. 5. Thermal resistance vs time for a 28.8mm gate width GaN HEMT.

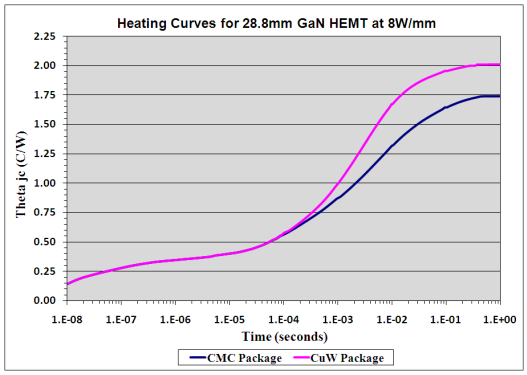

Fig. 6. Transient response of 28.8mm gate width GaN HEMT in two different packages.

V. AMPLIFIER DESIGN EXAMPLES

When designing power amplifiers it is important that the transistors operate below their rated operating junction or channel temperatures thus ensuring that the amplifier will have the desired reliability as predicted by the relevant device process Arrhenius plot. Since many of today's amplifier designs are performed using large signal models in harmonic balance simulators those models need to be able to predict device channel temperatures for any given output power level and associated power added efficiency (PAE). A thermal "engine" has been implemented within Cree's large-signal models. An example of using this self-heating large-signal model is in the design of a Doherty amplifier where two transistors are operated in very different modes. The carrier amplifier in a Doherty configuration runs in a CW mode up to the point where the peaking amplifier takes over. After this point the carrier amplifier is held at saturation at its maximum efficiency. With modulated signals the power dissipation is

often as low as 2W/mm. The peaking amplifier, operating in Class C or even F, is only active when the RF input signal is large enough to turn the transistor "on" - it will only be turned on at the peaks of the modulated signal and is essentially operating in a transient mode. Since the two transistors in a Doherty amplifier are thermally isolated from one another they are assigned different thermal resistance numbers to ensure correct prediction of junction temperatures. The resulting temperature performance of the carrier and peaking amplifiers as a function of RF power is shown in Fig. 7. The effect of introducing a transient thermal resistance for the peaking amplifier, which is one third the value used for the carrier amplifier, is shown. This emulates the effective pulse width and duty factor of a typical W-CDMA signal. To better display the difference in the self-heating we have also used transistors operated at 48 volts at 7 watts/mm of gate periphery at peak power. The dark traces show the simulation of channel temperatures in the two transistors if CW thermal resistance were assumed. The light traces show the result when the peaking amplifier employs a transient thermal resistance. It is clear when the peaking amplifier starts to turn-on and the effect it has on keeping the carrier amplifier's temperature relatively constant. The red curve shows the channel temperatures of an "equivalent" balanced amplifier.

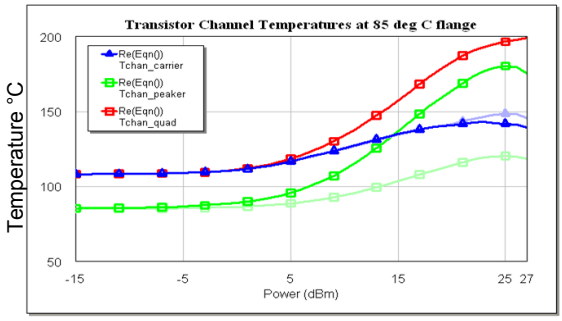

Fig. 7. Channel temperatures of carrier and peaking amplifiers in 850 MHz, 100 watt Doherty Amplifier.

Wide bandgap transistors, due to their intrinsic properties, are also finding many applications in wide bandwidth high power designs where efficiency is one of the most critical parameters. In these circuits, the use of accurate thermal resistance values is essential. Small errors in the value of thermal resistance can make the difference between a successful design and one that has poor reliability due to excessive channel temperature. In the design of these amplifiers simulations are made of small signal performance where the power dissipation (Pdiss) is very low (~1W/mm) and full large signal performance where Pdiss can be as high as 8W/mm depending on the efficiency and operating voltage. To be able to simulate gain compression as a function of drive power accurately the thermal model needs to be non-linear in itself as already described in section III. Fig. 8 shows the effect that an accurate thermal model has on a high power amplifier's large signal performance compared with no thermal model. Note particularly the degradation in high power gain and PAE for a device operating at 42 volts on its drain optimally matched (harmonically) at 2.45 GHz.

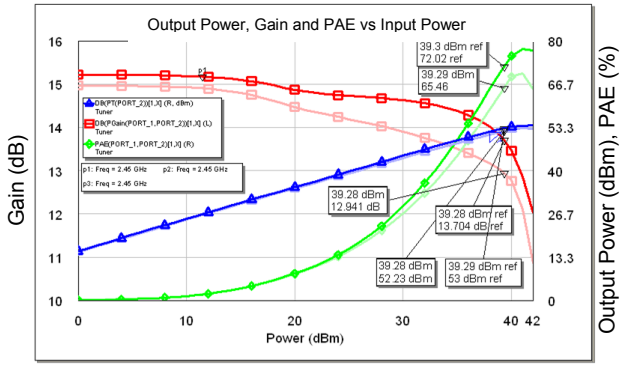

Fig. 8. Impact of channel temperature on the RF performance of a high efficiency 2.45 GHz PA.

VI. CONCLUSIONS

When designing power amplifiers it is important to pay attention to the thermal performance of the transistor and its impact on RF performance and reliability of the resulting amplifier. Since wide bandgap power transistors are capable of operating at much higher power densities compared to other semiconductor technologies it is even more important to ensure that the correct thermal resistance of a given transistor and system environment is available. It has been shown that careful IR spectroscopy measurements coupled with accurate, correlated, finite element analyses provide thermal resistances for a large range of operating conditions. The effects of non-linear thermal resistance modeling have then been applied to design examples using RF CAD software with self-heating large signal models. The resulting amplifier designs using this approach have been proven to be robust, stable and take full advantage of all of the aspects of the GaN HEMT on SiC materials system.

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