Abstract—A comprehensive method of designing a broadband Doherty power amplifier is presented in this paper. The essential limitations of bandwidth extension of a Doherty power amplifier are discussed based on the proposed structure of the Doherty power amplifier, which also takes the output matching networks of both sub-amplifiers into account. The broadband matching is realized by applying the simplified real frequency technique with the desired frequency dependent optimum impedances. GaN transistors were selected to implement the circuit structure.

Index Terms—Doherty power amplifier, broadband, systematic design procedure, real frequency technique.

I. INTRODUCTION

MODERN wireless communication systems, such as WiMAX, W-CDMA, UMTS and LTE, introduce the amplitude modulation to enhance the data transmission rate and maximize the bandwidth efficiency in the provided limited frequency band [1]. However, their associated high peak-to-average power ratio constrains the power amplifiers working at a sufficient back-off power level to ensure the acceptable linearity, which is at the expense of efficiency [2]. The Doherty amplifier employing active load-pull modulation is considered to be a very promising solution to enhance the efficiency over a large back-off power region. Linearization techniques have been utilized to improve the linearity properties [3], [4]. Broadband Doherty power amplifiers have been reported recently [5]–[10]. Both the quarter-wave impedance transformer and the output capacitance of the transistors were considered as the limiting factors of the bandwidth extension in the broadband Doherty power amplifier design [7]. Parallel inductors were introduced to compensate the output capacitances of the transistors for a broadband real impedance transformation. Nevertheless, the resulting LC resonant circuits possess small bandwidth that in turn limits the bandwidth of the Doherty power amplifier. Assuming ideal transistors without output capacitors, Bathich has reported the mathematical analysis of a broadband Doherty power amplifier in [8], which reveals that the impedance inverter has a great influence on the bandwidth extension at both the back-off and saturation power levels. However the influence of the peaking power amplifier at the back-off power level was not included in the analytical model. Up to the author’s knowledge, all the analysis of a broadband Doherty power amplifier reported in the previous works are based on the simplified classical Doherty model proposed by Cripps [2] without considering the package, the bias tee nor the output matching networks. All these disregarded factors will be discussed in detail in this paper. Re-optimization of the output matching networks contributes to the bandwidth extension of the broadband Doherty power amplifier.

The real frequency technique was primarily introduced by Carlin [11] and further developed by Yarman [12], [13]. It employs a nonlinear optimization simulator for the optimum matching solution over a given frequency band. Aksen represented his methods of constructing the matching networks using lumped elements together with the transmission lines in the design of microwave amplifiers in his dissertation [14]. A designed S-Band broadband GaN power amplifier by applying the real frequency technique has been reported in [15].

In this paper, the real frequency technique for solving broadband double matching problems is briefly introduced. The bottlenecks of the Doherty power amplifier’s bandwidth extension are discussed in detail. Design methods of the broadband Doherty power amplifier are presented: The sub-amplifiers are constructed respectively followed by an assembly, which fulfills several necessary conditions derived from the vector analysis. Doherty power amplifiers were implemented with equal size GaN HEMT transistors to validate the proposed methods.

II. THEORETICAL ANALYSIS OF THE BROADBAND DOHERTY AMPLIFIER

A. Real frequency technique for the double-matching problem

The frequency dependent property of an ideal lossless reciprocal two-port network is described by its scattering matrix in the Belevitch canonic form [16] as:

\[
S = \begin{bmatrix}
\frac{h(p)}{f(p)} & \frac{f(p)}{g(p)} \\
\frac{n(f(-p)/f(p))/g(-p)}{h(-p)/g(p)} & \frac{h(-p)}{g(p)}
\end{bmatrix}
\]

(1)

where \(h(p), f(p)\) and \(g(p)\) are polynomials of variable \(p = j\omega\) as:

\[
h(p) = h_0 + h_1p + h_2p^2 + \ldots + h_np^n
\]

(2)

\[
f(p) = f_0 + f_1p + f_2p^2 + \ldots + f_np^n
\]

(3)

\[
g(p) = g_0 + g_1p + g_2p^2 + \ldots + g_np^n
\]

(4)
g is a strictly Hurwitz polynomial [17], \( f \) is a real monic polynomial and \( \sigma = f(-p)/f(p) \) is a unimodular constant. The polynomials \( h \), \( f \) and \( g \) are related by the losslessness requirement [14]:
\[
g(p)g(-p) = h(p)h(-p) + f(p)f(-p)
\] (5)
where \( \max\{\deg(h),\deg(f)\} \leq \deg(g) \).

Fig. 1 illustrates a two-port network \([N]\) doubly terminated with the frequency dependent load impedances \(Z_C\) and \(Z_L\). The transducer power gain is defined in terms of the scattering parameters of \([N]\) as [14]:
\[
T(p) = \frac{(1 - |S_G|^2)(1 - |S_L|^2)}{1 - S_G S_L^*}\frac{(1 - S_G^2)|S_1|^2 (1 - S_L^2)}{1 - S_{11} S_G^2 |1| S_{22} + \frac{S_G^2 S_G}{(1-S_{11} S_G^2)} S_L^2 |1| (1 - S_L^2)} g(p) - h(p) S_G + S_L (h(-p) - S_G g(-p))^2
\] (6)

An LC low-pass filter is employed as the optimization prototype, so that \( f(p) \) is simplified to a constant value, namely \( f(p) = 1 \). Based on the knowledge of \( S_C \) and \( S_L \), the components’ values in the LC filter are optimized by applying Levenberg-Marquardt Algorithms for the transducer power gain as high and as flat as possible over the given frequency interval. In particular, if either \( S_C \) or \( S_L \) is frequency independent, the double-matching problem degenerates into a single-matching problem.

### B. Necessary and sufficient conditions of assembling sub-power amplifiers for the Doherty working principle

The carrier power amplifier works in coordination with the peaking power amplifier to realize the Doherty working principle. The respective designs of both sub-amplifiers followed by an assembly is desired to simplify the Doherty power amplifier design procedure. The peaking power amplifier with an equal size transistor can not deliver the desired amount of power at the saturation power level, which equals to that from the carrier amplifier. Therefore, the ideal load modulation is not realizable. The broadband Doherty power amplifier can be optimized at either the back-off or the saturation power level according to the design specifications, termed as "optimization at the back-off power level (option I)" and "optimization at the saturation power level (option II)" respectively. Option I (II) implies that the optimum modulated impedance of the carrier power amplifier can be only achieved at the back-off (saturation) power level, while the modulated impedance at the saturation (back-off) power level assumes only a suboptimum value due to the non-ideal load modulation. As depicted in Fig. 2(c) and Fig. 3(d), the output matching network of the Doherty power amplifier consists of three two-port networks \([S_C]\) ([\( \{S_{C1}\} \), \( S_P \) and \( S_L \)], whose frequency properties are described by their associated scattering parameters \([S_{C1}]\) ([\( \{S_{C1}\} \), \( S_{P} \) and \( S_{L} \)], \( Z_{opt,C,H} \) and \( Z_{opt,P,H} \) denote the optimized impedances of the carrier and the peaking power amplifiers at the saturation power level respectively. \( Z_{opt,C,L} \) and \( Z_{opt,P,L} \) are defined as the corresponding desired impedances respectively. \( Z_{PT,r} \) is the impedance looking into the transistor drain node under the cold-FET condition. \( Z_{PT,r,L} \) represents the impedance looking into the peaking power amplifier at the junction, when the peaking transistor doesn’t work. The systematic design procedures for both options will be discussed respectively.

#### 1) Optimization at the back-off power level (option I):

The load impedance \( R_0 \) is transferred to \( Z_{L,J} \) via a two-port network \([S_L]\). \( Z_{PT,r,L} \) is assumed to possess frequency dependent scattering parameter equidistantly placed on the edge of the 50 Ohm normalized Smith chart with \(-45^\circ < \arg\{S_{PT,r,L}\} < 45^\circ \) (quasi-open-circuit impedance [29]) over the desired frequency band. The resulting impedance \( Z_{C,J,L} \) is matched to \( Z_{opt,C,L} \) via a two port network \([S_C]\) applying by the real frequency technique with \( Z_{D,C,L} \) as the optimization goal. The ABCD-matrix of \([S_C]\) is defined as:
\[
ABCD_C = \begin{bmatrix} A_C & B_C \\ C_C & D_C \end{bmatrix}
\] (7)

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At the saturation power level, the frequency dependent impedance $Z_{opt,C,H}$ associated with drain efficiency $\eta_{C,H}$ and output power $P_{C,H}$ of the carrier power amplifier is subjectively selected based on the loadpull simulation and measurement results. With the knowledge of $Z_{opt,C,H}$, the impedance $Z_{C,I,H}$ is obtained as:

$$Z_{C,I,H} = \frac{D_c \cdot Z_{opt,C,H} - B_c}{A_c - C_c \cdot Z_{opt,C,H}} \tag{8}$$

The modulated impedances of both sub-amplifiers looking into the combination junction are calculated as:

$$Z_{C,I,H} = Z_{L,J} \cdot (1 + \frac{P_{P,H}}{I_{p,H,I,J}}/I_{C,I,H}) = Z_{L,J} \cdot (1 + \frac{P_{P,H}}{I_{p,H,I,J}}) \tag{9}$$

$$Z_{P,I,H} = Z_{L,J} \cdot (1 + \frac{P_{P,H}}{I_{p,H,I,J}}/I_{p,H,I,J}) = Z_{L,J} \cdot (1 + \frac{1}{\frac{P_{P,H}}{I_{p,H,I,J}}}) \tag{10}$$

which can be further rearranged as:

$$\frac{P_{P,H}}{I_{p,H,I,J}} = \frac{Z_{C,I,H}}{Z_{L,J}} - 1 \tag{11}$$

$$Z_{P,I,H} = Z_{L,J} \cdot (1 + \frac{1}{\frac{P_{P,H}}{I_{p,H,I,J}}}) = Z_{C,I,H}/\frac{P_{P,H}}{I_{p,H,I,J}} \tag{12}$$

The powers delivered into the junction are computed as:

$$P_{C,H} = \Re\left\{ \frac{I_{p,H,I,J} \cdot V_{I,J,I}}{2} \right\} = \frac{\sqrt{V_{I,J,I}} \cdot \Re(\Phi_{Z_{C,I,H}})}{2} \tag{13}$$

$$P_{P,H} = \Re\left\{ \frac{I_{p,H,I,J} \cdot V_{I,J,I}}{2} \right\} = \frac{\sqrt{V_{I,J,I}} \cdot \Re(\Phi_{Z_{P,I,H}})}{2} \tag{14}$$

The desired power delivered by the peaking power amplifier is obtained as:

$$P_{P,H} = \frac{\sqrt{V_{I,J,I}}}{\Re(\Phi_{Z_{P,I,H}})} \cdot \frac{\Re(\Phi_{Z_{C,I,H}})}{\Re(\Phi_{Z_{C,I,H}})} \cdot P_{C,H} \tag{15}$$

If minimum drain efficiency $\eta_{D,H}$ of the Doherty system is required over the specific frequency band, the minimum drain efficiency provided by the peaking power amplifier $\eta_{P,H,min}$ is calculated as:

$$\eta_{P,H,min} = \frac{P_{P,H}}{(P_{C,H} + P_{P,H})/\eta_{D,H} - P_{C,H}/\eta_{D,H}} \tag{16}$$

The selection of $S_{opt,C,H}$ should fulfill the following requirements:

- The frequency dependent drain efficiency at the saturation power level $\eta_{C,H}$ should be as flat and as high as possible.
- The resulting desired output power of the Doherty system $P_{C,H} + P_{P,H}$ should be as flat and as high as possible.
- Since the modulated impedance $Z_{P,I,H}$ must be passive in the working frequency range, $S_{opt,C,H}$ should be selected in the frequency dependent stable modulation’s area (details in appendix A).

The broadband Doherty design method based on the back-off power level optimization is demonstrated in Fig.2 and explained as follows:

- $[S_L]$ is constructed to transfer $R_0$ to a low impedance $Z_{L,J}$ over the working frequency range. The desired impedance $Z_{D,C,L}$ associated with the maximum achievable drain efficiency $\eta$ is determined through the harmonic balance simulation at each frequency point $f_1$ within the specified frequency range. Assuming

the “quasi-open-circuit” impedance $Z_{PT,r,I,J}$, $Z_{C,I,I}$ is obtained based on the knowledge of $Z_{L,J}$, $Z_{D,C,L}$ and $Z_{C,I,I}$ are employed as the generator and load impedances in the nonlinear optimization for solving the double matching problem. As illustrated in Fig.2(a), the two port network $[S_C]$ is optimized, so that the transducer power gain T defined in (6) is as flat and as high as possible. Since the circuit involves the active nonlinear transistor, a further optimization is necessary to achieve the drain efficiency as flat and as high as possible over the specified frequency range by applying the ADS optimization and harmonic balance simulator.

- The desired frequency dependent load modulation’s destination $S_{opt,C,H}$ is subjectively selected at the saturation power level, that in turn enables the calculation of $Z_{C,I,H}$, $\hat{K}$ and $Z_{P,I,H}$.

- The carrier amplifier is simulated with the frequency dependent complex load impedance $Z_{C,I,H}$ at the saturation power level. $\eta_{C,H}$, $P_{C,H}$ and $I_{C,I,H}$ at the load termination $Z_{C,I,H}$ are determined through the harmonic balance simulation. $\eta_{P,H,min}$ and $P_{P,H}$ are calculated through (15) and (16).

- The peaking power amplifier is simulated with the load termination $Z_{P,I,H}$. $Z_{P,I,H}$ is transferred to $Z_{opt,P,H}$ via the two-port network $[S_P]$. The two-port network $[S_P]$ is optimized, so that the transistor delivers flat output power around $P_{C,H}$ with the minimum drain efficiency $\eta_{P,H,min}$ over the given frequency interval. Moreover, the quasi-open-circuit requirement on $Z_{PT,r,I,J}$ is also included as an optimization’s boundary of constructing $[S_P]$.

- The current $I_{P,I,H}$ is simulated at the load termination $Z_{P,I,H}$ of the peaking power amplifier. The phase difference between $I_{C,I,H}$ and $I_{P,I,H}$ is adjusted to equal to the phase of $\hat{K}$ by tuning the electrical lengths $\theta_{C0}$ and $\theta_{P0}$ of phase compensation lines, as depicted in Fig. 2(b).

- Both respectively designed sub-amplifiers are assembled at the saturation power level. All the circuit parameters are adjusted to achieve the best performance of the broadband Doherty power amplifier, as illustrated in Fig.2(c).

2) Optimization at the saturation power level (option II):

If the broadband Doherty power amplifier is to be optimized at the saturation power level, both $Z_{C,I,H}$ and $Z_{P,I,H}$ assume real impedance values, which implies that $\hat{K}$ degenerates to a frequency dependent real value over the specified frequency range. Therefore, according to (15) the current modulation coefficient $K$ is derived as:

$$K = \frac{I_{P,I,H}}{I_{C,I,H}} = \frac{P_{P,H}}{P_{C,H}} \tag{17}$$

The modulated impedances at the saturation power level are calculated as follows:

$$Z_{C,I,H} = Z_{L,J} \cdot (1 + \frac{P_{P,H}}{P_{C,H}}) \tag{18}$$

$$Z_{P,I,H} = Z_{L,J} \cdot (1 + \frac{P_{C,H}}{P_{P,H}}) \tag{19}$$

The design procedure of a broadband Doherty power amplifier optimized at the saturation power level is illustrated in Fig. 3
(a) Respective design and optimization of the carrier and peaking power amplifiers at the saturation power level

(b) Determination of the common load impedance $Z_{L,J}$, the modulated impedances $Z_{P,J,H}$ and $Z_{C,J,H}$ and the characteristic impedance and phase of the impedance inverter

(c) Re-optimization of the output matching work of the carrier amplifier at the saturation power level to compensate the influence of the impedance inverter

(d) Assembly of the Doherty power amplifier at the back-off power level

Fig. 3. Block diagram explaining the design procedure associated with the saturation optimization method (option II).

C. Limitations of the Doherty power amplifier bandwidth extension

Several aspects limit the bandwidth extension of the Doherty power amplifier, which are either related to the general
broadband matching limitation theory or associated with the Doherty working mechanisms.

![Diagram of broadband matching problem due to the transistor package.](image)

Fig. 4. Broadband matching problem due to the transistor package.

1) General limitation of broadband matching: Bode and Fano have introduced the limitations of broadband matching problems based on mathematical analysis [18], [19]. In this paper, the limitation is discussed graphically in the Smith chart. According to the conventional analysis method of a power amplifier proposed by Cripps [2], as illustrated in Fig. 4, the optimum impedance $Z_{opt,in}$ at the transistor intrinsic current generator plane PO-PO' possesses a frequency independent value, which is determined by the current and voltage boundaries of the selected transistor and the power amplifier working principle (for example, class B, E, J). Since any physically realizable circuit component introduces positive phase dispersion (defined in Appendix B), the desired impedance at the P2-P2' plane $Z_{opt,D}$ exhibits negative phase dispersion, which is observed from both the loadpull simulation and measurement results. The load impedance $Z_L$ is transferred by the output matching network to $Z_{imp,L}$, with which the transducer power gain is optimized as high and as flat as possible over the specified frequency range. Generally, the resonance frequency of the transistor’s package is highly above the working frequency range. If assuming that the output matching network does not introduce any resonance over the given frequency interval, both $Z_{imp,L}$ and $Z_{opt,D}$ are smooth arcs with opposite phase dispersion polarities. The increasing frequency directions are indicated by the increasing frequency values, as $F_{0,x} \leq F_{1,x} \leq F_{2,x} \leq F_{3,x} \leq F_{4,x}$ with $x$ denoting the names of the curves. In Fig. 5(a), both arcs intersect only once at frequency $F_2$, represented by the coincidence of $F_{2,A1}$ and $F_{2,A2}$. The frequency dependent angle $\gamma$ (defined in Appendix B) between both instantaneous normal vectors is always greater than 90°, that implies the narrow-band matching only around $F_2$. Otherwise, as illustrated in Fig. 5(b), a resonance is deliberately introduced around $F_2$ within the given frequency range. During part of the resonance, $\gamma$ becomes smaller than 90°, that enables the broadband matching over the specified frequency range. Generally, the broadband matching is limited by:

$$Z_{opt,D} = \frac{Z_0 R_0 + j \frac{Z_0}{\sqrt{2}} \tan \beta L}{\sqrt{2} \frac{Z_0}{\sqrt{2}} + j R_0 \tan \beta L}$$ (20)

$$Z_{C,J} = \frac{Z_{L,J} (1 + \frac{I_{P,J} H}{I_{C,J} H})}{2Z_{L,J}}$$ (21)

$$Z_{L,J} = \frac{Z_{C,J} + j Z_0 \tan \beta L}{Z_0 + j Z_{C,J} \tan \beta L}$$ (22)

The influences of the impedance inverter over the specified frequency range is included in the frequency dependent

![Graphical explanation of the bandwidth limitation](image)

Fig. 5. Graphical explanation of the bandwidth limitation

2) Influence of the impedance inverter: Up to now, the $\lambda/4$ transmission line impedance inverter is asserted as the bottleneck of the bandwidth extension in the broadband Doherty power amplifier design and implementation. Actually, its influence can be compensated by the output matching network of the carrier amplifier by investigating the impedance transformation in Fig. 6. In Fig. 6(a), $Z_{L,1}$ represents the frequency dependent input impedance looking into the impedance inverter with $\beta = 90^\circ$ at the center frequency. Assuming an ideal load modulation at the saturation power level, namely $I_{C,J,H} = I_{P,J,H}$, the impedances over the specified frequency range from 2.3 GHz to 2.9 GHz at the saturation power level are obtained as:

The complexity of the desired impedance terminations $S_G$ and $S_L$ in Fig. 1 (Analytical proof in [20]).

The maximum number of components allowed in the matching networks.

The realizable values of the components in the working frequency range: Lumped components are limited by their associate self resonance frequencies. Distributed microstrip lines are limited by the range of the implementable line width.

- The complexity of the desired impedance terminations $S_G$ and $S_L$ in Fig. 1 (Analytical proof in [20]).

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- The complexity of the desired impedance terminations $S_G$ and $S_L$ in Fig. 1 (Analytical proof in [20]).

- The maximum number of components allowed in the matching networks.

- The realizable values of the components in the working frequency range: Lumped components are limited by their associate self resonance frequencies. Distributed microstrip lines are limited by the range of the implementable line width.
impedance $Z_{L,1}$. In contrast, in Fig. 6(b), $Z_{L,2}$ possesses a frequency independent impedance $R_0$. $Z_{opt,D}$ represents the desired optimum impedance associated with the maximum drain efficiency at the saturation power level over the given frequency range, which are simulated with the GaN transistor CGH40006P large signal model at the reference plane directly following the bias tee, as depicted in Fig.4 and Fig. 6. Both impedances $Z_{L,1}$ and $Z_{L,2}$ are to be transferred to the desired impedance $Z_{opt,D}$ to achieve the highest flat drain efficiency over the specified frequency range. Output matching networks OMN$_{C1}$ and OMN$_{C2}$ are optimized respectively from 2.3 GHz to 2.9 GHz by applying the real frequency technique (double matching problem). The LC low-pass filter prototype is employed in the optimization. The optimized matching networks containing two stage LC filters and the associated resulting impedances $Z_{imp,L,1}$ and $Z_{imp,L,2}$ are demonstrated together with the desired impedance $Z_{opt,D}$ in Fig. 7(a) and Fig. 7(b) respectively. The optimized components in the LC prototype are different for the both cases. However, extremely small differences between the resulting impedances $Z_{imp,L,1}$ and $Z_{imp,L,2}$ looking into both output matching networks can not be distinguished. Provided with “the same” implemented impedances $Z_{imp,L,1} \approx Z_{imp,L,2}$, the transistor will deliver “the same” performance for both cases. Therefore, the influence of the impedance inverter, represented by the frequency dependence of the impedance $Z_{L,1}$, is compensated by and absorbed into the output matching network. The same conclusion can be also derived from the optimization results by applying the three stage LC filter structure, as illustrated in Fig. 8. Better matching solutions are achieved. However, the resulting unrealistic components labeled with red color are difficult to be implemented over the microwave frequency range.

3) Bandwidth limitation due to the quasi-open-circuit requirement on $Z_{PTR,J,L}$:

- Up to the back-off power level, the peaking power amplifier does not work. The impedance $Z_{PTR}$ looking into the transistor at the cold-FET condition is transferred to $Z_{PTR,J,L}$ at the junction via $|S_P|$. Ideally, $Z_{PTR,J,L}$ has an infinite impedance to prevent power leakage up to the back-off power level [30], which was assumed in the analysis by Bathich [9]. However, actually, $Z_{PTR,J,L}$ lies on the edge of the Smith chart. The phase of $Z_{PTR,J,L}$ is controlled within the range $[-45^\circ, 45^\circ]$ to fulfill the quasi-open-circuit requirement. Any realizable component in the peaking power amplifier output path introduces positive phase dispersion into $Z_{PTR,J,L}$, which in turn degenerates the maximum achievable bandwidth of the Doherty power amplifier. Therefore, any component excluding the output matching network should be avoided between the peaking transistor and the junction $J$.

4) Bandwidth limitation associated with the optimization methods:

- If the broadband Doherty power amplifier is optimized at the given back-off power level, the bandwidth extension of the Doherty system is determined by the general

Fig. 7. Optimization of the output matching networks (two stage LC structure) to compensate the influence of the impedance inverter.

Fig. 8. Optimization of the output matching networks (three stage LC structure) to compensate the influence of the impedance inverter.
broadband matching theory on the construction of \([S_C]\) and the quasi-open-circuit requirement on \(Z_{PTr,J,L}\) at the back-off power level. Moreover, at the saturation power level, the subjective selection of the frequency dependent \(S_{C,J,H}\) determines \(\eta_{C,H}\). \(P_{C,H}\) and \(Z_{P,J,H}\). Several optimization boundaries are applied for constructing \([S_P]\), labeled with red color in Fig. 2(b), as follows:

- \(Z_{opt,P,H}\) is transferred from \(Z_{P,J,H}\) via the to be optimized two-port network \([S_P]\). Provided with \(Z_{imp,P,H}\), the transistor should deliver a flat output power around the calculated value \(P_{H}\) with the minimum drain efficiency of \(\eta_{P,H,min}\).
- \(Z_{PTr,J,L}\) transferred from \(Z_{PTr}\) at the back-off power level must fulfill the quasi-open-circuit requirement at the back-off power level.

Nonlinear optimization with several boundaries presents difficulty in providing feasible solutions over a broad frequency band [21].

- If the broadband Doherty power amplifier is optimized at the saturation power level, \(Z_{C,inv,H}\) is optimized around 50 Ohm at the saturation power. Inserting a section of transmission line with \(Z_{CT} = 50 \text{ Ohm}\) characteristic impedance will not change the matching condition at the saturation power level (see Fig. 3(d)). Increasing the electrical length \(\theta_{CT}\) at the center frequency results in clockwise rotation of the impedance \(Z_{C,invT,H}\) starting from \(Z_{C,inv,H}\) around the origin in the 50 Ohm normalized Smith chart. Larger \(\theta_{CT}\) also leads to more positive phase dispersion, since the wavelength is frequency dependent and inversely proportion to the frequency. On the other hand, the desired frequency dependent load modulation’s destination is the impedance associated with the maximum drain efficiency over the specified frequency range at the back-off power level, which exhibits negative phase dispersion over the given frequency range. For example, the optimum impedance associated with the maximum drain efficiency at the back-off power level, evaluated at the output of the constructed carrier power amplifier output matching network (OMN), is illustrated in Fig. 9 (simulation results with CGH40006P GaN transistor large signal model). In contrast, any realistic impedance \(Z_{C,inv,H}\) or \(Z_{C,invT,H}\) possesses positive phase dispersion, that implies the impossibility of an ideal broadband matching. At the back-off power level, \(\theta_{CT}\) can be adjusted and optimized either for the explicit drain efficiency enhancement over a relatively small frequency range (version I) or for maximum achievable flat drain efficiency over a wide frequency band (version II). As illustrated in Fig. 3(d), since the matching condition at the saturation power level is not changed by increasing \(\theta_{CT}\), both versions provide the same performance. The simulated impedances of \(Z_{C,invT,H}\) at the output of the matching network for both cases are illustrated in Fig. 9.

### III. IMPLEMENTATION AND MEASUREMENT OF THE BROADBAND DOHERTY AMPLIFIER

To verify the proposed ideas in Section II, Cree GaN CGH4000P transistors are selected to implement the symmetrical broadband Doherty power amplifier with the center frequency at 2.6 GHz. As for the broadband Doherty power amplifier based on back-off power level optimization, the strict optimization boundaries imposed on the construction of \([S_P]\), which are determined by the subjective choice of \(Z_{opt,C,H}\), always result in unacceptable performance. Therefore, this paper focuses solely on the design option II.

#### A. Circuit design and implementation

Primarily, the transistor drain side package model is obtained by applying the method of Franco Giannini [22]. The
carrier power amplifier was designed at the operating point of $V_{DS} = 28$ V, $I_{DS} = 40.41$ mA. The optimum source impedance changes along with the increasing input power due to the nonlinearity of $C_{GS}$ and $C_{GD}$. Assuming the tuned-load termination at the intrinsic current generator plane, the frequency dependent optimum source impedances $Z_{C,S}$ is obtained for the maximum drain efficiency at the saturation power level. By applying the real frequency technique, 50 Ohm is transferred to $Z_{C,S}$ with a desired transducer power gain $T$ greater than 0.9 over the design frequency range. The second harmonic impedance is employed to improve the efficiency of the carrier amplifier over the specified frequency range [23], [24]. Second harmonic loadpull simulations at the reference plane P1-P1’ in Fig. 4 were performed at the transistor drain node by applying the optimum fundamental impedances associated with the maximum output power at the saturation power level, where the third harmonic impedances were set to 50 Ohm. The optimum second harmonic impedance exhibits anticlockwise rotations (negative phase dispersion) with the increasing frequency, as illustrated in Fig. 10. The second harmonic load impedance affects both the DC and fundamental components of the current and voltage obtained from the nonlinear simulation [25]. The output power is saturated and changes little, while more than 8% drain efficiency improvement can be achieved due to the decrease of the DC current by applying an appropriate second harmonic load termination. The modified drain bias circuit is employed in the carrier power amplifier design, as depicted in Fig. 11 and Fig. 12, which introduces less positive phase dispersion over the second harmonic frequency range. The peaking power amplifier is constructed at the bias point of $V_{GS} = -5.8$ V, $V_{DS} = 28$ V. Its bias tee is placed at the junction point, where $Z_{L,J}$ in Fig. 3(d) possesses a low impedance in the frequency range, so that the influence of $Z_{PTP,J,L}$ is minimized (see Fig. 11 and Fig. 12). The DC block capacitor of the peaking power amplifier is shifted and placed just in front of the output SMA connector. All broadband matching networks are optimized based on the knowledge of optimum impedances via the real frequency technique. The same topology is employed for both carrier and peaking power amplifiers for an easy phase compensation of both PA paths over the design frequency band. The optimum components in the LC low-pass filters are replaced with microstrip lines at the center frequency of 2.6 GHz [26]. The Rogers RF substrate 4350B with $\varepsilon_r = 3.66$ and $H = 0.762$ mm is utilized to fabricate the circuit layouts, which were optimized through the electromagnetic simulation by applying the ADS Momentum harmonic balance co-simulation. The electrical length $\theta_{CT}$ in Fig. 3(d) was adjusted for the broadband Doherty power amplifier version I, which exhibits explicit efficiency enhancement over the band $2.4 - 2.9$ GHz, and for the version II, that provides more than 40% drain efficiency at the 5 – 6 dB output power back-off level between $2.2 – 3.0$ GHz, as depicted in Fig. 11 and Fig. 12.

**B. Measurement results**

The scattering parameters of the fabricated broadband Doherty power amplifiers were measured under their nominal bias points, namely $(I_{DS,C} = 41.41$ mA, $V_{GS,P} = -5.8$ V and $V_{DS,C} = V_{DS,P} = 28$ V). The measurement results (with solid lines) and the simulation results (with dashed lines) are reported in Fig. 13 and Fig. 14 respectively. Differences in $S_{22}$ between both versions have been observed due to the different electrical lengths $\theta_{CT}$ of the phase compensation lines. Continuous wave (CW) signals were applied to characterize the drain efficiency and output power performance. Fig. 15 presents the measured drain efficiency at the saturation and the 5 – 6 dB back-off power levels of both broadband Doherty power amplifiers (Version I and II), while the associated measurement results of the output power are given in Fig. 16.
The measured drain efficiency on dependence of the output power is presented in Fig. 17 and Fig. 18. The measured gain with respect to the input power is reported in Fig. 19 and Fig. 20. The linearity properties of the fabricated Doherty power amplifiers were evaluated by measuring the third-order inter-modulation (IMD3) characteristic by applying two-tone signals with 5 MHz frequency spacing in the

Fig. 15. Measured and simulated drain efficiency at the saturation and the 5-6 dB back-off output back-off power levels with CW signal.

Fig. 16. Measured and simulated output power at the saturation and the 5-6 dB back-off output back-off power levels with CW signal.

Fig. 17. Measured drain efficiency of the broadband Doherty power amplifier (Version I) with CW signal.

Fig. 18. Measured drain efficiency of the broadband Doherty power amplifier (Version II) with CW signal.

Fig. 19. Measured gain of the broadband Doherty power amplifier (Version I) with CW signal.

Fig. 20. Measured gain of the broadband Doherty power amplifier (Version II) with CW signal.

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Fig. 21. Measured upper-band third-order inter-modulation (IMD3) of the broadband Doherty power amplifier (Version I) with two-tone signal.

Fig. 22. Measured lower-band third-order inter-modulation (IMD3) of the broadband Doherty power amplifier (Version I) with two-tone signal.

Fig. 23. Measured upper-band third-order inter-modulation (IMD3) of the broadband Doherty power amplifier (Version II) with two-tone signal.

Fig. 24. Measured lower-band third-order inter-modulation (IMD3) of the broadband Doherty power amplifier (Version II) with two-tone signal.

Fig. 25. Measured gain, drain efficiency and PAE with WiMAX signal at 2.6 GHz.

IV. CONCLUSION

The bandwidth limitations of a Doherty power amplifier have been discussed with considering the output matching networks of both sub-amplifiers by applying the real-frequency technique. It reveals the generalized and novel bottlenecks for the bandwidth extension in a broadband Doherty power amplifier design. Design methods of broadband Doherty power amplifiers have been presented with the introduced current modulation factor $\vec{K}$ for both optimization methods. The classical Doherty power amplifier’s topology was modified to mitigate the optimization’s requirements on constructing the peaking power amplifier. Two versions of broadband Doherty power amplifier have been designed and fabricated.
The performance of the fabricated broadband Doherty power amplifiers (Version I and II) are compared with those in the previous publications in Table I. The frequency band, over which the drain efficiency greater than 40% can be obtained at the 5 – 6 dB back-off power level, is utilized for the performance evaluation of the broadband Doherty power amplifiers. Version I exhibits explicit drain efficiency enhancement from 2.3 to 2.8 GHz, while Version II provides drain efficiency higher than 40% over the frequency range from 2.2 to 2.9 GHz at the 5 – 6 dB output power back-off power level. Up to the author’s knowledge, the presented measurement performances of the broadband Doherty power amplifiers in this paper are among the highest ones with equal size transistors. Moreover, the works proposed by Bathich [9], [10] utilize SMD capacitors in the broadband matching networks. The self resonance frequency of commercial available SMD components limits their application in the microwave circuit design. The production tolerance will generally result in unpredictable deviations between the simulation and measurement results, that in turn presents difficulties in the post tuning procedure. In this work, microstrip transmission lines are employed in the design, which overcomes these problems. No post-tuning is necessary during the measurements because of the accurate performance prediction with the ADS co-simulation. Acceptable nonlinearity characteristics have been measured, which can be further improved applying digital predistortion techniques.

### Table I

<table>
<thead>
<tr>
<th>Index</th>
<th>Specification</th>
<th>Frequency Range</th>
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<th>Year</th>
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<tr>
<td>[5]</td>
<td>NA</td>
<td>2.5-2.7</td>
<td>GaN</td>
<td>2007</td>
</tr>
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<td>2.5-2.7</td>
<td>HIT</td>
<td>2010</td>
</tr>
<tr>
<td>[7]</td>
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<td>1.7-2.1</td>
<td>LDMS</td>
<td>2010</td>
</tr>
<tr>
<td>[8]</td>
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<td>1.65-2.25</td>
<td>GaN</td>
<td>2010</td>
</tr>
<tr>
<td>[9]</td>
<td>40% DE</td>
<td>1.7-2.6</td>
<td>GaN</td>
<td>2011</td>
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<td>GaN</td>
<td>2011</td>
</tr>
<tr>
<td></td>
<td>Version II</td>
<td>2.2-2.96</td>
<td>GaN</td>
<td>2011</td>
</tr>
</tbody>
</table>

* Simulation results.
* Uneven Doherty (Different transistors).
* At 6-7 dB output power back-off level (OBO).
* At 5-6 dB output power back-off level (OBO).
* Direct input power splitting.

### Appendix A

**STABILITY CIRCLE DEFINITION FOR THE CASE OF BACK-OFF OPTIMIZATION DESIGN METHOD**

\[ S_{\text{opt},C,H}, S_{C,J,H} \text{ and } S_{L,J} \text{ are the S parameters of } Z_{\text{opt},C,H}, \\
Z_{C,J,H} \text{ and } Z_{L,J} \text{ with the norm impedance } Z_0. \]

\[ S_{\text{opt},C,H} = \frac{Z_{\text{opt},C,H} - Z_0}{Z_{\text{opt},C,H} + Z_0} = \frac{S_{c11} + S_{c12}S_{C,J,H}}{1 - S_{c22}S_{C,J,H}} \]

\[ S_{C,J,H} = \frac{Z_{C,J,H} - Z_0}{Z_{C,J,H} + Z_0} = \frac{(S_{opt,C,H} - S_{c11})S_{c22} + S_{c12}S_{c21}}{Z_0} \]

Then the current modulation coefficient \( \tilde{\kappa} \) is obtained as:

\[ \tilde{\kappa} = \frac{Z_{C,J,H}}{Z_{L,J}} - 1 = \frac{1 + S_{\text{opt},C,H}(1 - S_{L,J})}{1 - S_{\text{opt},C,H}(1 - S_{L,J})} - 1 \]

Further, the desired load impedance \( Z_{P,J,H} \) of the peaking power amplifier looking into the combination junction at the saturation power level can be represented in terms of \( S_{\text{opt},C,H} \), calculated as:

\[ Z_{P,J,H} = \frac{Z_{C,J,H} - Z_0}{\tilde{\kappa}} = \frac{3S_{L,J} + S_{C,J,H}S_{L,J} - S_{C,J,H}}{3S_{C,J,H} + S_{C,J,H}S_{L,J} - S_{L,J} + 1} \]

\[ = \frac{A \cdot S_{\text{opt},C,H} + B}{C \cdot S_{\text{opt},C,H} + D} \]

with:

\[ A = S_{L,J} - 1 + (1 + 3S_{L,J}) \cdot S_{c22} \]
\[ B = -S_{c11}(S_{L,J} - 1 + (1 + 3S_{L,J}) \cdot S_{c22}) + (1 + 3S_{L,J})S_{c12}^2 \]
\[ D = -S_{c11}(S_{L,J} + 3 + (1 - S_{L,J}) \cdot S_{c22}) + (1 - S_{L,J})S_{c12}^2 \]
\[ C = S_{L,J} + 3 + (1 - S_{L,J}) \cdot S_{c22} \]

As for the impedance \( Z_{P,J,H} \), its scattering parameter should be limited in the area for the feasible implementation of the broadband matching network. Under the assumption of \( |S_{P,J,H}| < \alpha \), the impedance \( Z_{\text{opt},C,H} \) should be selected out of the circle described by its center \( c \) and radius \( r \) [28]. Specially, \( \alpha = 1 \) represents the stable boundary of \( S_{P,J,L} \).

\[ c = \frac{\alpha^2 c^* D - A^* B}{|A|^2 - \alpha^2 |C|^2} \]

\[ r = \sqrt{|A|^2 - \alpha^2 |C|^2} \]

### Appendix B

**DEFINITION OF PHASE DISPERSION WITHIN A GIVEN FREQUENCY RANGE**

Fig. 27 illustrates three convex curves representing frequency dependent impedances in the Smith chart, where the arrows indicate the increasing frequency directions. \( \beta \), in Fig. 27(a), helps to determine the increasing frequency direction.
It’s defined as the phase between the instantaneous tangential vector at \( F_0 \) and the vector starting from the scattering parameter at \( F_0 \) to that at \( F_0 + \Delta F \) in the Smith chart. As in Fig. 27(a), the direction of the instantaneous tangential vector is so defined that it always fulfills \( \lim_{\Delta F \to 0} \cos(\beta) > 0 \), where \( \Delta F \) is a small frequency step. \( \alpha \) represents the phase starting from the positive horizontal direction to the tangential vector in clockwise direction. Under the assumption of two frequency points \( F_1 \) and \( F_2 \) with \( F_2 > F_1 \), the phase increment at frequency \( F_1 \) is defined as:

\[
d\alpha(F_1) = \lim_{F_2 \to F_1} (\alpha_2 - \alpha_1)
\]

(30)

For convex curves, \( d\alpha \) possesses the same polarity in the frequency range \([F_1, F_2]\). The phase dispersion \( \Psi \) of the impedance in the given frequency range \([F_1, F_2]\) is calculated as:

\[
\Psi = \int_{F_1}^{F_2} d\alpha(F)
\]

(31)

where \( F \) is located in the frequency range \([F_1, F_2]\). Fig. 27(b) and Fig. 27(c) describe two impedance curves possessing the same pattern with different increasing frequency directions. The phase dispersion of the impedance represented by the curve in Fig. 27(b) is positive, while the phase dispersion of the other is negative.

The unit normal vector is \( 90^\circ \) behind the tangential vector (clockwise), as illustrated in Fig. 27. \( \gamma \) represents the phase between instantaneous unit normal vectors of two curves at the same frequency point, with \( 0^\circ \leq \gamma \leq 180^\circ \). Fig. 27(d) illustrates the instantaneous phase \( \gamma_1 \) and \( \gamma_2 \) between the curves B and C at frequency points \( F_1 \) and \( F_2 \). The frequency dependent \( \gamma \) over the specified frequency range is employed for estimating the feasibility of a broadband matching.

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REFERENCES


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