# New Output Combiner for Doherty Amplifiers

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***Abstract*—In this letter, a new output combining network for the implementation of a Doherty Power Amplifier (DPA) is presented. The proposed topology simultaneously allows the active load modulation and the output matching, by adopting more realizable elements than the standard DPA, especially when high output power levels are required. The innovative design approach is demonstrated through a practical prototype realization based on GaN-HEMT devices. Experimental results have shown a 65%–48% efficiency at about 42–36 dBm output power with a gain compression lower than 1.5 dB from 1.95 to 2.25 GHz.**

***Index Terms*—Doherty power amplifier (DPA), GaN, WiMAX.**

## I. Introduction

THE Doherty power amplifier (DPA) operating principle is based on the idea to modulate the output load of a Main active device by using the current generated by an Auxiliary active device [1]. In order to properly exploit this active load modulation, an impedance inverter network (IIN) has to be interposed between the output load [$R_L$ in Fig. 1(a)] and the Main device [1]. Moreover, an impedance transforming network (ITN) is frequently required to match the DPA to the standard output termination, usually 50 Ω. In the standard DPA topology both the IIN and the ITN are typically implemented with a quarter-wave transmission line ($\lambda/4$-TLine), by adopting the topology in Fig. 1(a) [2]–[4]. Recent papers demonstrated the possibility to improve either the DPA bandwidth by using the Real Frequency Technique [5] or the average efficiency by implementing a multi-stage architecture [6]. In both cases, the adopted output combiner is an improved version of the standard one. The aim of this contribution is to demonstrate that the functionalities of the IIN and the ITN can be implemented by adopting the network reported in Fig. 1(b). As can be noted, it is similar to a branch-line coupler except for the termination at the fourth port [$P_4$ in Fig. 1(b)]. In fact, the standard resistive termination is removed, leaving an open circuit condition at that port. It will be demonstrated that, the proposed solution allows more feasible characteristic impedances of the transmission lines, as compared as to the standard approach, especially when high output power levels are required. Implementations of DPAs based on hybrid couplers as output power combiner have previously been proposed in [7]. However, that solution still maintains the necessity of an output matching network (OMN) for each active device and a further offset line between the OMN and the output combiner. The solution proposed here allows to remove these two networks, leading to a higher level of integration, wider bandwidth and lower losses.

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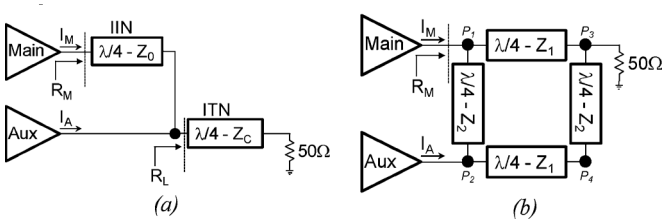


Fig. 1. (a) Typical and (b) proposed DPA implementation.

## II. Analysis of the Proposed Output Power Combiner

The proposed combiner, reported in Fig. 1(b), is composed by four $\lambda/4$-TLines. The horizontal $\lambda/4$-TLines have equal characteristic impedance $Z_1$. The vertical $\lambda/4$-TLines have equal characteristic impedance $Z_2$. Analyzing the network in Fig. 1(b), the following relationship can be derived for the load ($R_M$) seen by the Main device:

$$R_M = \frac{Z_1^2}{50\ \Omega}\left(\frac{Z_2^2}{Z_1^2 - Z_2^2}\right)^2 + \frac{I_A}{I_M}\frac{Z_1^2}{Z_2}\left(\frac{Z_2^2}{Z_1^2 - Z_2^2}\right) \quad (1)$$

where $I_M$ and $I_A$ are the fundamental currents of the Main and Auxiliary devices, respectively. Moreover, it has been assumed that $I_M$ lags $I_A$ by 90°, as used in the classical DPA configuration. When the Auxiliary device is turned off, the current $I_A$ is zero. Consequently, $R_M$ is equal to the first factor of the sum in (1), depending only on $Z_1$ and $Z_2$. When the Auxiliary is turned on, the current $I_A$ is greater than zero. Therefore, if $Z_2 > Z_1$, the second factor of the sum in (1) assumes a negative value, reducing $R_M$. As a consequence, the active load modulation is properly performed. In particular, by assuming

$$Z_1^2 = Z_2^2\left(1 - \frac{Z_2}{100\ \Omega}\right) \quad (2)$$

the condition $R_{M,(IA=0)} = 2 \cdot R_{M,(IA=IM)}$ is obtained from (1), as required for a DPA having 6 dB of output power back-off (OBO) [1]. It is essential to stress that (2) shows a physical limitation for the possible values given by $Z_2 < 100\ \Omega$.

The behaviors of $Z_1$ and $Z_2$ as a function of $R_M$ at the saturation, i.e., when $I_A = I_M$, can be derived by using (1) and (2). The resulting curves are plotted in Fig. 2. In the same figure are also reported the behaviors of $Z_0$ and $Z_C$ that should be used in a classical DPA topology, to obtain the same $R_M$ value.

As can be noted, the implementation of a standard DPA could be critical if $R_M < 20\ \Omega$, due to the extremely low values required for $Z_0$ and $Z_C$. Conversely, the proposed combiner maintains reasonable values of $Z_1$ and $Z_2$ also with $R_M$ in the neighborhood of 5 Ω. Low values of $R_M$ are usually required

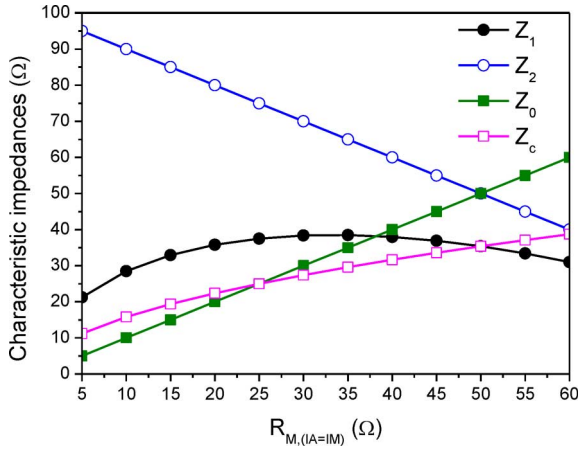


Fig. 2. Behaviors of the characteristic impedances of the $\lambda/4$-TLines in the proposed combiner and in the standard approach.

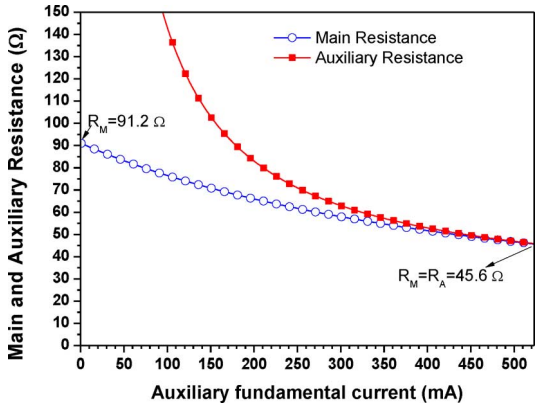


Fig. 3. Devices' loads as a function of the Auxiliary current.

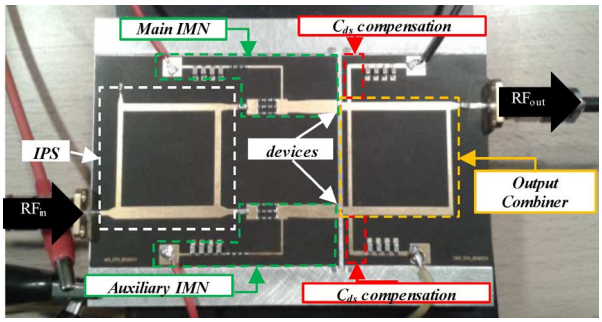


Fig. 4. Photo of the realized DPA.

when high levels of current, and thus output power, have to be achieved. As a consequence, the proposed combiner demonstrates a suitable advantage with respect to the standard approach for the implementation of high power DPAs. In fact, by assuming the same drain bias voltage, a $R_M = 5\ \Omega$ allows to reach four times higher output power than a $R_M = 20\ \Omega$.

In the actual design, the optimum loads for the Main and Auxiliary devices at the break and saturation points depend on both the physical limits of the used active devices and the maximum output power ($Pout|_{Max}$) and OBO levels of the DPA [1]. To this purpose, the $Pout|_{Max}$ and OBO values were selected to be 41 dBm and 6 dB, respectively. Commercial GaN HEMTs (Cree CGH60008D) are used as active devices [8]. According to the device data sheet, the drain bias voltage is set to 28 V. The correspondent maximum current ($I_{max}$) and knee voltage ($V_k$) to fulfill the selected $Pout|_{Max}$ and OBO values are 1.3 A and 4 V, respectively. The center frequency of the DPA was chosen to be 2.1 GHz. Once these boundary conditions are selected, all the other DPA design parameters can be estimated [1]. The resulting optimum load of both active devices at the saturation is $R_{M,(IA=IM)} = R_{A,(IA=IM)} = 45.6\ \Omega$, due to the selected $OBO = 6$ dB. As a consequence, the load of the Main device at the break point is double ($R_{M,(IA=0)} = 91.2\ \Omega$). Finally, the amplitude of the fundamental current component of the Auxiliary device at the saturation was estimated to be $I_{1A} = 523$ mA. Thus, $Z_1 = 36.6\ \Omega$ and $Z_2 = 54.1\ \Omega$ are derived by using (1) and (2). In order to verify the load modulation concept, these values of $Z_1$ and $Z_2$ were implemented in the proposed combiner and a simulation was performed to estimate the behaviors of $R_M$ and $R_A$ as a function of the current $I_A$. As it can be noted from Fig. 3, the active load modulation is verified. In fact, the output load of the Main device is modulated from 91.2 Ω to 45.6 Ω while the output load of the Auxiliary device starts from an open circuit, becoming equal to 45.6 Ω at the saturation.

## III. DPA Design and Experimental Results

In order to validate the new output combiner, a prototype was designed on a commercial substrate: Roger Duroid 5880 ($H = 381$ um, $T = 17$ um, $\varepsilon_r = 2.2$). The active devices have been connected to the input (IMN) and output (OMN) matching networks by using three bond wires ($D = 25$ um, $L = 900$ um) for each connection. The photography of the realized DPA is shown in Fig. 4.

For the design, the following steps were carried out:

1) The output combiner was designed according to the results obtained in the previous section.
2) The output capacitance of each device was compensated by using a short circuit stub ($C_{ds}$ compensation in Fig. 4). The same element is used to bring the drain bias voltage as well.
3) The IMN of each active device (Main IMN and Auxiliary IMN in Fig. 4) was designed to assure both the unconditional stability and a resistive input load condition. In particular, the impedances seen at the input of the Main and Auxiliary branches are synthesized to be about 30 Ω.
4) The uneven input power splitter (IPS in Fig. 4) was designed to fulfill the required power splitting ratio ($P_{in,Aux}/P_{in,Main} = 1.15$ dB). This level of splitting ratio was firstly theoretically estimated as described in [1] and then optimized by using the nonlinear model of the active device. A branch-line coupler was preferred for the design of the IPS, since it automatically allows the compensation of the phase between the two amplifiers' paths, i.e., the driving conditions to assure that $I_M$ lags $I_A$ by 90° has previously assumed to derive (1). Moreover, the Branch-line coupler is preferable since it allows an uneven power division on equal impedance values ($Z_{in,M} = Z_{in,A} = 30\ \Omega$). Conversely, the solutions based on the Wilkinson divider does not allow an uneven splitting on equal impedances without losses [9].

Fig. 5 shows the Continuous Wave (CW) measured performances at 2 GHz for the nominal bias point ($V_{DD} = 28$ V,

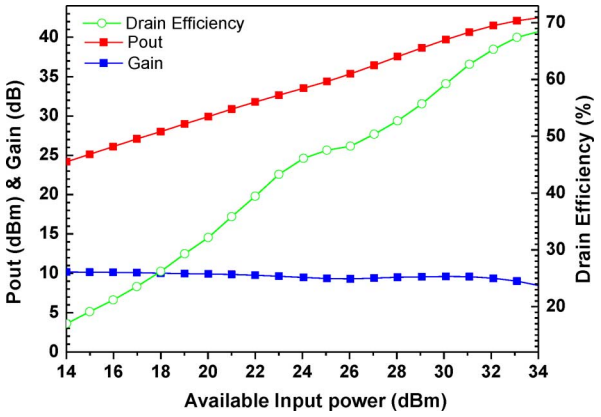


Fig. 5. CW measured performances versus input power at 2 GHz.

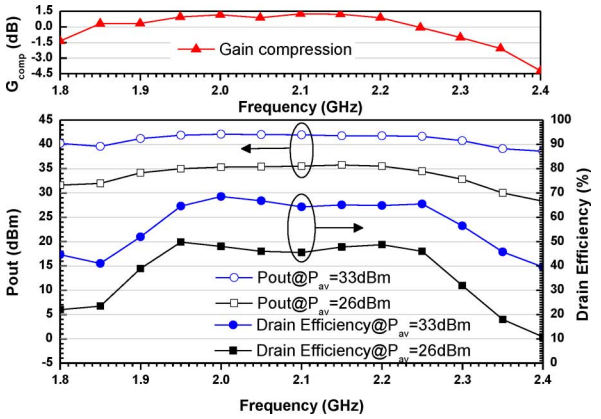


Fig. 6. CW measured performances versus frequency at 33 dBm of input power.

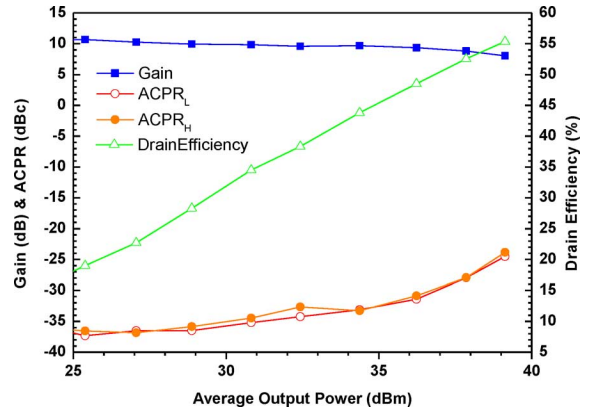


Fig. 7. WiMAX measured performances at 2.1 GHz.

$V_{GG,Main} = -2.63$ V and $V_{GG,Aux} = -5$ V). In particular, an output power level around 42 dBm has been obtained at 33 dBm of available input power ($P_{av}$), with a related efficiency of about 68 %. Moreover, the efficiency is higher than 48 % in the 6 dB of OBO range (i.e., for $P_{av} = 26$ dBm) with a gain compression of about 1.5 dB only.

Fig. 6 shows the DPA performances versus frequency for a constant available input power level of 33 dBm and 26 dBm, respectively. As it can be noted, 65 %–48 % of efficiency at about 42–36 dBm of output power have been measured from 1.95 to 2.25 GHz. In the whole 300 MHz bandwidth, the gain compression is lower than 1.5 dB. Finally, the DPA has also been tested using a WiMAX signal with 8.8 dB PAPR and 5 MHz bandwidth around 2.1 GHz [10].

Fig. 7 shows the measured Low and High Adjacent Channel Leakage Ratio ($ACLR_{L/H}$), average efficiency and gain behaviors as a function of the average output power. At 37 dBm output power, the average efficiency is around 50 % with $ACLR_{L/H}$ values lower than $-30$ dBc. The experimental results confirm the potentiality of the proposed solutions, showing performances that are in-line with already published DPA realizations in the S-band [11].

## IV. Conclusion

In this letter, a new topology to implement a DPA was presented. In the new circuit configuration, the IIN and the ITN functions are realized and integrated in a symmetrical output combiner that allows a greater feasibility with respect to the standard approach. Experimental results have shown an output power of 42 dBm with an efficiency of 65 % from 1.95 to 2.25 GHz in CW operative mode. 50 % of average efficiency and $-30$ dBc of ACPR have been demonstrated driving the DPA with a 5 MHz-WiMAX signal.

## References


[1] P. Colantonio, F. Giannini, R. Giofrè, and L. Piazzon, "The AB-C Doherty amplifier, Part I: Theory," *Int. J. RF Microw. CAE*, vol. 19, no. 3, pp. 293–306, May 2009.

[2] P. Colantonio, F. Giannini, R. Giofrè, and L. Piazzon, "The AB-C Doherty power amplifier. Part II: Validation," *Int. J. RF Microw. CAE*, vol. 19, no. 3, pp. 307–316, May 2009.

[3] J. Kim, J. Son, J. Moon, and B. Kim, "A Saturated Doherty power amplifier based on saturated amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 2, pp. 109–111, Feb. 2010.

[4] S. A. Bassam, X. Li, Y. Liu, K. Rawat, M. Helaoui, F. M. Ghannouchi, and Z. Feng, "Design and linearization of concurrent dual-band Doherty power amplifier with frequency-dependent power ranges," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 10, pp. 2537–2546, Oct. 2011.

[5] G. Sun and R. H. Jansen, "Broadband Doherty power amplifier via real frequency technique," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 1, pp. 99–111, Jan. 2012.

[6] M. W. Lee, S.-H. Kam, Y.-S. Lee, and Y.-H. Jeong, "Design of highly efficient three-stage inverted Doherty power amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 7, pp. 383–385, Jul. 2011.

[7] R. E. Mayer, K. W. Lho, L. F. Root, and E. W. Louis, "High Efficiency Amplifier," U.S. Patent 6.922.102 B2, Jul. 26, 2005.

[8] Cree CGH60008D Datasheet [Online]. Available: http://www.cree.com available on

[9] P. Colantonio, F. Giannini, and E. Limiti, "Power combining," in *High Efficiency RF and Microwave Solid State Power Amplifiers*. Hoboken, NJ: Wiley, 2009, pp. 370–434.

[10] Agilent Technologies, WiMAX (IEEE 802.16-2004) 89600 Vector Signal Analysis Software Feb. 2011, Appl. Note 5989-2029EN.

[11] R. Giofrè, L. Piazzon, P. Colantonio, and F. Giannini, "Being seventy-five still young: The Doherty power amplifier," *Microw. J.*, vol. 55, no. 4, pp. 72–88, Apr. 2012.