A GaN HEMT Power Amplifier with Variable Gate Bias for Envelope and Phase Signals

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***Abstract* - This paper describes the design, simulation and measurement of a GaN power amplifier suitable for envelope and phase signal combination. The low-frequency envelope signal is used to vary the gate (bias) voltage of the device, resulting in a pulse width modulated drain voltage, while modulation of supply voltage or current is avoided. The test circuit is implemented using a discrete GaN HEMT power amplifier and discrete surface-mount passive components assembled on a PCB. Measurements showed a maximum drain efficiency of 59% at 360 MHz, at an output power of 29 dBm. The output power as a function of the gate bias voltage varied between 3 and 29 dBm, with the drain efficiency varying between 6 and 59%.**

I. Introduction

Some of the challenges of modern telecommunication systems are power consumption and performance of the transmitter. Communication systems develop towards higher frequencies, larger bandwidths, higher transmit output power and larger peak-to-average ratios, while user handsets and base stations at the same time are operating for multiple standards. Thus, the transmitter linearity requirements become more stringent. Due to increased performance requirements in both handsets and base stations, power consumption is an issue for both components, as cooling is an increasingly costly factor of base stations and battery lifetime is a well-known factor of handsets.

The power amplifier is a critical component in the transmitter; A typical class-A solution will provide linearity but will lead to high power consumption in order to meet performance requirements. Therefore, many architectural solutions have been investigated and implemented, such as Envelope Elimination and Restoration (EER), Envelope Tracking (ET), Linear Amplification with Non-Linear Components (LINC), etc [1-5]. On the circuit design level, an increased interest in switch-mode power amplifiers (PA) has been shown, also at radio frequencies [3, 6, 7].

In this paper we present a power amplifier architecture suitable for a transmitter using separated envelope (low-frequency) and phase (high-frequency) signals (see Fig. 1). The PA is switch-mode, and both the low- and high-frequency signal operate on the gate of the GaN HEMT; The envelope drive signal controls the gate bias signal, which is a low level signal and so there is no need for a switch mode amplifier as is required for systems using drain voltage modulation, and no modulation of the supply voltage or current occurs.

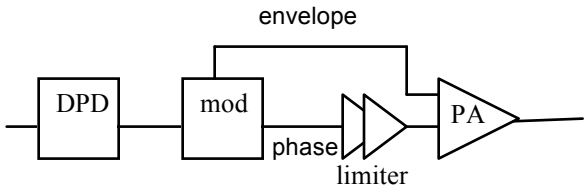


Fig. 1. Transmitter architecture.

It is well known that modern modulation schemes such as W-CDMA and OFDM require very linear amplification. Unfortunately, this amplifier structure is designed for efficiency and is far from linear, so some form of linearization will be required before the signal splitter stage. Digital Predistortion (DPD) [9] would be a potential candidate for this as it can handle wide bandwidths and memory effects can also be included.

The signal separator that splits the envelope and phase components is best done using envelope tracking techniques to avoid the spectrum expansion on the phase modulated drive signal. Overdriving the driver amplifier feeding the PA can remove the modulation on this waveform.

The transmitter may be implemented by having the predistorter, modulator and limiter on a single chip, driving the power amplifier.

Because of practical limitations, and having the goal of testing this PA concept in mind, the operating frequency of the power amplifier is designed to be 400 MHz. This is done by choosing suitable discrete component values for the input and output tuning network. The discrete GaN HEMT device is chosen in order to achieve a high output power and a high efficiency in switch-mode. The full amplifier including matching networks is implemented using surface mount components on a standard FR4 PCB, with double sided copper layers.

In section 2 of this paper the amplifier design is described, and in section 3 simulation and measurement results are presented. Conclusions are drawn in section 4.

I. Circuit Design

As mentioned in the Introduction, the envelope (low-frequency) signal is used to effectively change the bias level at the gate of the device. The phase (limited, high-frequency) signal thus causes the transistor to be switched on for a shorter or longer length of time, as illustrated in Fig. 2. This results in a pulse-width modulated signal at the drain of the device. This signal is then filtered by the output tuning network, giving a variation in output power, as desired.

The PA is shown in Fig. 3. The output tuning network provides filtering of the square-wave drain voltage signal and performs impedance transformation from the load impedance to the drain of the device. The networks were optimized and fine-tuned in order to accomodate a range of pulse widths by simulations using the harmonic balance simulation in ADS.

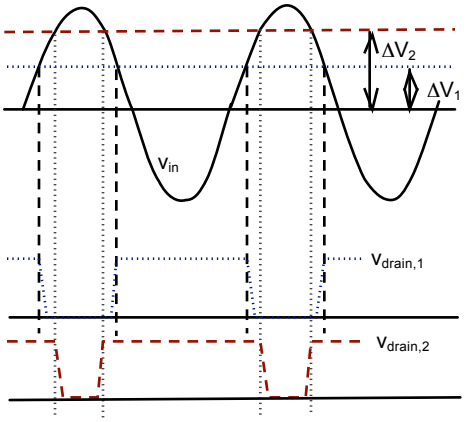


Fig. 2. Operating principle of the power amplifier. The difference Δv between V_{bias} and V_{th} varies, depending on V_{bias}, and the resulting pulse width modulated drain voltage is illustrated for two cases.

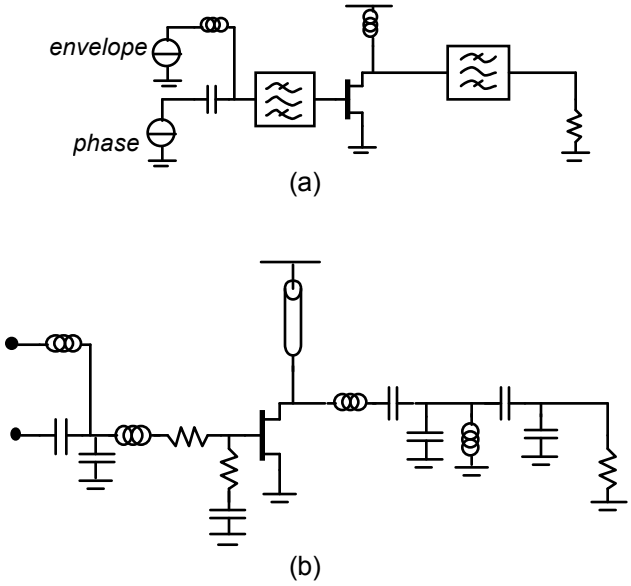


Fig. 3. Power amplifier schematic, (a). Block diagram, (b). Implementation.

The inductor at the drain of the device is implemented through a transmission line on the PCB, giving an inductance of approximately 0.6 nH at 400 MHz. All other passive components are surface mounted on the PCB.

The device is a Cree CGH40010 discrete GaN HEMT device suitable for high output power (typically 13W at P_{-3dB}) and high efficiency (60% at P_{-3dB}). The threshold voltage is typically -2.5 V, and the specified supply voltage is 28 V [8]. In our measurement setup we limited the supply voltage to 10 V, due to practical considerations.

The original modulated baseband signal is restored at RF at the output of the PA, as the variable gate bias level combines with the constant-envelope high-frequency signal. The output network to some extent provides filtering of the desired output frequency band. It must be noted that the characteristic from the low-frequency signal to the output is non-linear; It is assumed that pre-distortion [9] or feedback [10] is used.

I. Results

A. Simulation results

The power amplifier was simulated using the harmonic balance simulation in ADS. The transmission line and other PCB traces were taken into account as well. Simulations showed a maximum drain efficiency of 78% at 400 MHz, at an output power of 34.5 dBm, and a maximum output power of 38.5 dBm at 450 MHz (see Fig. 4) for a supply voltage of 18 V, V_{bias} of -3 V and the amplitude of the input voltage at 10 V.

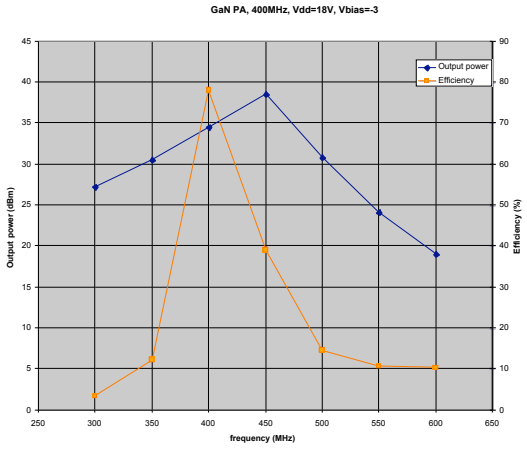


Fig. 4. Simulation results for $V_{d\,d}$ = 18 V, $V_{in,peak}$ = 10 V and V_{bias} = -3 V.

For a variation of V_{bias} from -1.5 to -7 V, the output power varies from 35.7 to 8.4 dBm, while the efficiency varies from 86.4 to 8.4%.

A supply voltage of V_{dd} = 10 V will according to simulations give a drop in output power of approximately 5 dB while maintaining the same level of efficiency.

B. Measurement results

The circuit was assembled on the PCB (see Fig. 5), and a

high-power input signal was used, since the PA was to operate in switch-mode. A spectrum analyzer was used to measure the output signal.

The maximum drain efficiency is reached for an input frequency of 360 MHz (see Fig. 6(a)), and the maximum output power for a frequency of 400 MHz. For a supply voltage of V_{dd} = 5 V and a gate bias voltage of V_{bias} = -2.8 V, the maximum drain efficiency is 58%, with an output power of 22 dBm, and the maximum output power is 26 dBm.

For a supply voltage of 10V and V_{bias} of -2.6 V, a drain efficiency of 56% was achieved at a frequency of 360 MHz, with an output power of 28 dBm. In Fig. 6(b) the efficiency and output power as a function of V_{bias} are shown.

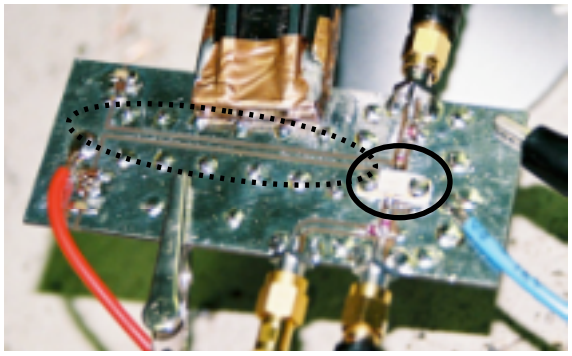


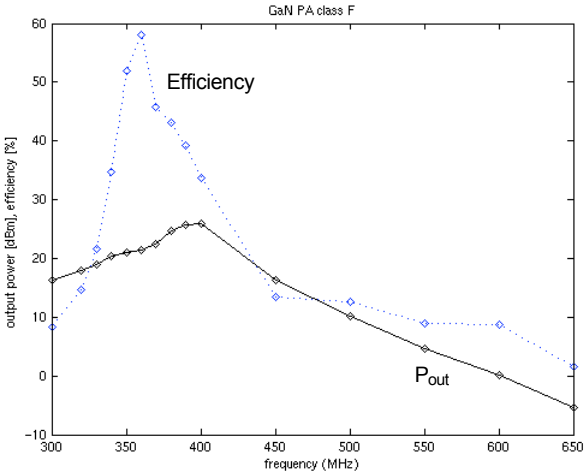
Fig. 5. The PCB with the transmission line indicated by the dashed ellipse and the device by the solid one.

Figure 6(b) shows that the useful range of gate bias voltage variation is roughly 2.5 V, from -4 to -1.5V. This results in an output power variation from 3 to 29 dBm, and a drain efficiency variation from 6 to 59%. For a supply voltage of V_{dd} = 5 V the efficiency was slightly higher (maximum 60%) and the output power lower (maximum 23 dBm).

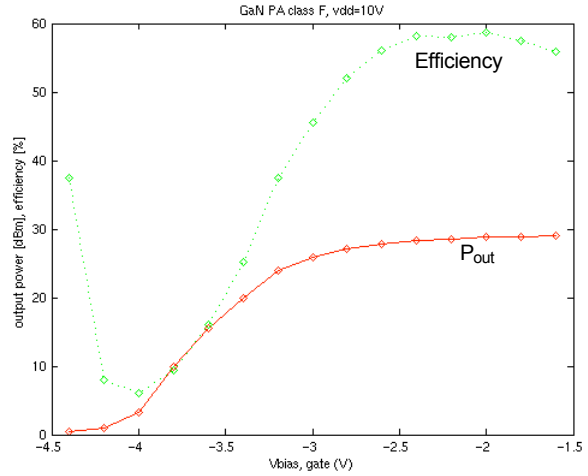
The deviation in operating (maximum efficiency) frequency may be due to slight differences in transmission line characteristics, as well as the presence of parasitic capacitance that was not fully taken into account in simulations. The reduced maximum drain efficiency may be due to the non-ideality of passive componenets, such as the inductors having a limited quality factor, and the PCB traces and soldering having a small impedance.

For a similar variation in output power and efficiency as was simulated, the bias voltage variation is much smaller, that is, 2.5 V compared to 5.5 V. This may be due to non-idealities in the input tuning network.

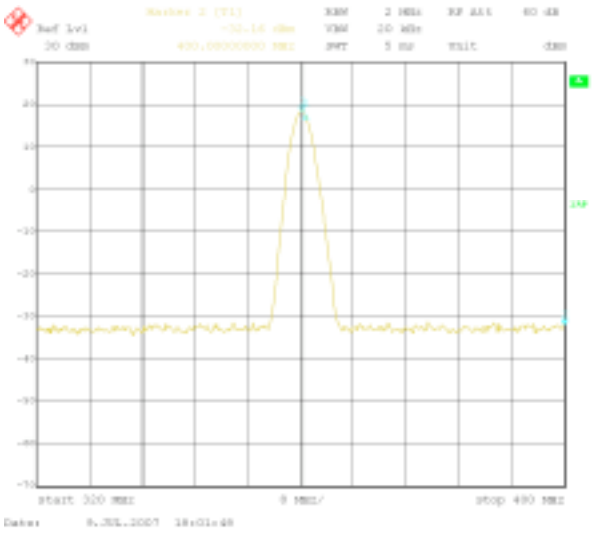
The measurement results are summarized in Table I.



(a)



(b)



(c)

Fig. 6. Measurement results, (a). Output power and drain efficiency for different frequencies, with V_{dd} = 5V, and V_{bias} = -2.8V, (b). Output power and drain efficiency as a function of gate bias voltage, with V_{dd} = 10V and f_{in} = 360MHz, (c). Spectral plot of the output power for V_{dd} = 10V and f_{in} = 360MHz, and V_{bias} = -2.4V. A 10dB attenuator was used.

TABLE I. SUMMARY OF MEASUREMENT RESULTS.

Parameter	Value	Comment
η_{max}	60%	Max. drain efficiency; Vdd = 5V, Vbias = -2.2 V, fin = 360 MHz
Pout @ η_{max}	23 dBm	Output power at max. drain efficiency
f0 @ η_{max}	360 MHz	Frequency of max. drain efficiency
P_{out} range	3 - 29 dBm	Vbias = -4 to -1.5 V;
η range	6 - 59 %	Vdd = 10 V, fin = 360 MHz

II. CONCLUSIONS

The design and measurement of a discrete power amplifier configuration was presented, utilizing a GaN HEMT device. The PA is suitable for an EER-like architecture where an envelope and phase signal are applied to the gate of the PA, thus avoiding modulation of the supply voltage or current. The envelope low-frequency signal is used to vary the bias level of the gate. The transmitter may be implemented on a single chip containing the predistorter, modulator and limiter, driving the discrete power amplifier.

The amplifier has input and output tuning networks that provide frequency selection and impedance transformation. The inductance at the drain of the device was implemented as a transmission line on the PCB. Measurements showed a maximum drain efficiency of 59% at 360 MHz, at an output power of 29 dBm.

The output power as a function of the gate bias voltage varied between 3 and 29 dBm, with the drain efficiency varying between 6 and 59%. Thus, a large variation in output power can be achieved without modulation of the supply voltage or current.

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