Evaluation of a GaN HEMT Transistor for Load- and Supply-Modulation Applications Using Intrinsic Waveform Measurements

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***Abstract*— In this paper, the efficiency of a GaN HEMT transistor and its intrinsic waveforms are measured at 0.9 GHz and investigated for load- and supply-modulation applications. The results show that both techniques perform equally well for back-off levels $\leq$6.5 dB. At higher back-off levels, the efficiency improvements achieved by supply modulation outperform load modulation. At 10 dB back-off, supply, and load modulation provide a power-added efficiency (PAE) of 68%, and 58%, respectively. Using measured intrinsic waveforms, it is shown that PAE degradations in load modulation can be mainly attributed to parallel losses rather than series losses, which are dominant in supply modulation. The harmonic contents of the intrinsic waveforms, in both techniques, are equally strong in back-off and peak power operations. There is, therefore, a great potential for further efficiency enhancement by circuit-level optimization of harmonic terminations for back-off.**

***Index Terms*— Efficiency, GaN HEMT, load modulation, power amplifier, supply modulation.**

I. Introduction

The efficiency of power amplifiers (PA's) with a fixed load impedance and supply voltage reduces at output power back-off. For a class-B PA, for example, the efficiency reduces from 78.5% at peak power to 24.8% at 10 dB back-off [1]. Therefore, the average efficiency for signals with high envelope variations becomes significantly lower than the maximum efficiency achieved at peak power.

Load- and supply-modulation techniques have recently shown to have a high potential in improving PA efficiency at back-off. In supply-modulation schemes, the output supply voltage (V_D) is dynamically controlled by an envelope amplifier (EA) and is reduced at lower output power (P_{out}) levels [2]. In load modulation, on the other hand, the PA load impedance is varied instantaneously by a varactor-based tunable matching network [3] or by the Doherty technique [4].

In [5], and [6], we used static measurements to evaluate the same LDMOS PA's in supply- and load-modulation schemes, respectively. The measurements were performed at the PA-output reference plane (50-Ω reference plane) and did not provide any detailed information about the device operation. No direct comparisons were made between the efficeicny results achieved in the two cases, and the loss mechanisms involved were not identified. In [2], the loss mechanisms of the transistor were investigated, merely, for supply-modulation applications. The importance of the harmonic terminations in back-off, when V_D is reduced, was also investigated but only based on simulations with transistor models.

In this paper, the efficiency performance and intrinsic waveforms of a GaN HEMT transistor are measured at 0.9 GHz to identify and compare the device intrinsic operation, dominant loss mechanisms, and the importance of harmonic terminations for PAE in back-off in load- and supply-modulation applications.

II. Measurement Procedure

The active multi-harmonic load-pull system presented in [7] is used for measurements. No source-pull is implemented at the fundamental or harmonic frequencies and a fixed impedance of approximately 50 Ω is used. The system measures voltage and current waveforms at the transistor package reference plane which is also the in-fixture calibration reference plane. An accurate model of the package parasitics and the connecting bondwires [8], makes it possible to de-embed the waveforms to the transistor reference plane. Finally, the approximate intrinsic waveforms at the transistor current-source reference plane can be extracted by de-embedding a constant drain-to-source capacitance (C_{ds}). This is a valid approximation for the GaN device under test (Cree CGH60015DE).

The measurement procedure is as follows: First, the fundamental load impedance (Z_L) and harmonic load impedances ($Z_{L,2f_0}$ and $Z_{L,3f_0}$) are optimized to reach maximum PAE at a P_{out} lower than 10 W, which is the maximum power limitation of the test setup employed. The drain bias voltage is 28 V and the gate bias is -2.6 V, which is slightly above the pinch-off voltage. Then, two cases are studied:

- Load modulation: Z_L is varied while $Z_{L,2f_0}$, $Z_{L,3f_0}$, and V_D are fixed. A power sweep is performed for each Z_L.

- Supply modulation: Z_L is kept fixed but V_D is varied. A power sweep is performed at each V_D.

The measurement results corresponding to each of the above cases are presented in the following two sections.

III. Load-Modulation Measurements

First, Z_L, $Z_{L,2f_0}$, and $Z_{L,3f_0}$ are optimized for maximum PAE at P_{out}=39 dBm. The PAE achieved at this P_{out} is 80%. No harmonic tuning source-pull capabilities were available in the measurement setup. This may explain the fact that the peak efficiency is slightly lower than expected. A fundamental load-pull and power-sweep experiment is then performed with the harmonic impedances and bias voltages fixed. The measured PAE results versus P_{out} are shown in Fig. 1. The dashed line shows the maximum achievable PAE at each P_{out} when the load modulation is applied. The optimum Z_L's are identified from the measured data and shown in Fig. 2, both at the transistor chip (bare-die) reference plane, and after de-embedding a constant C_{ds}=1.1 pF. In order to enhance the PAE in back-off by load modulation, a higher load resistance should be provided at lower P_{out}. The optimum susceptance, however, varies only slightly along this trajectory.

As shown in Fig. 1, although the PAE is significantly enhanced by load modulation, there is still a significant degradation compared to the peak PAE (80%). For example, the PAE is degraded from 80% at peak power to 58% at 10 dB back-off. These PAE degradations can not be explained by the series loss mechanism which is dominant in supply-modulation applications and is described by the following equation [2]:

$$\eta = \frac{\eta_{max}}{1 + \gamma_1 \frac{R_{on}}{R_{load}}}, \tag{1}$$

where η is drain efficiency and R_{load} is the real part of fundamental Z_L. γ_1 is a constant coefficient which is dependent on the waveform shapes but not P_{out}.

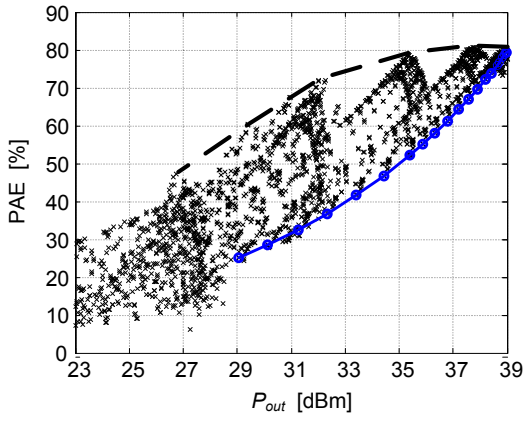

Fig. 1. Load-pull and power-sweep measurements at 0.9 GHz. Each $\times$ marker indicates a single measurement point corresponding to a certain Z_L and P_{in} combination. The solid line with $\circ$ markers shows the results when no load modulation is applied. The dashed line shows the maximum achievable PAE by load modulation.

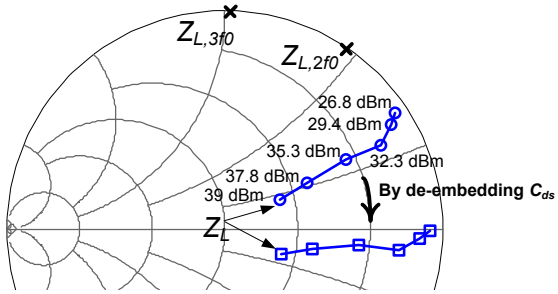

Fig. 2. Optimum Z_L versus P_{out}. Harmonic load impedances, after de-embedding C_{ds}, are shown by $\times$ markers.

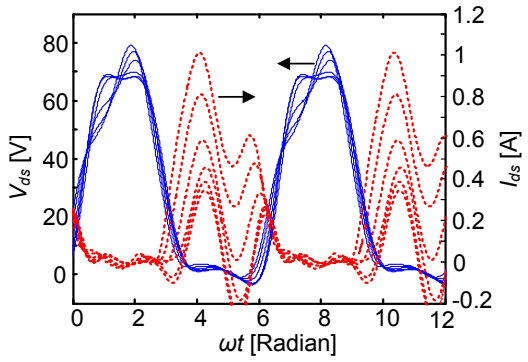

Fig. 3. Intrinsic waveforms of the transistor as power is backed off by load modulation according to the optimum Z_L's indicated by square markers in Fig. 2.

The series loss is associated with the on-resistance (R_{on}) and becomes the main loss mechanism for low V_D values [2], [9]. There are at least two arguements to explain why such a mechanism is not the main contributor to the losses when the load modulation is applied. Firstly, V_D is set high for peak power and is not reduced by load modulation. Secondly, the influence of R_{on} on efficiency decreases as R_{load} is increased. Since this is the case for load modulation when decreasing P_{out}, see Fig. 2, the series loss can not explain the efficiency degradations observed in load modulation.

Fig. 3 shows the measured waveforms at each of the optimum Z_L's indicated by square markers in Fig. 2. Note that the non-ideality of the waveforms is related to parasitics that exist inside the transistor model but were not de-embedded. However, the waveforms shown in Fig. 3 are still clear enough to give an insight to the intrinsic device operation. Clearly, by increasing the load resistance according to the optimal trajectory in Fig. 2, the current swing is decreased while the voltage swing is only slightly varied. The high and almost constant intrinsic voltage swing makes the parallel losses constant while the P_{out} is decreased by load modulation. As opposed to supply modulation, the PAE degradations are dominated by a parallel loss mechanism which can be expressed by the following equation:

$$\eta = \frac{\eta_{max}}{1 + \gamma_2 \omega^2 C_{ds}^2 R_P R_{load}}, \tag{2}$$

where R_P is an equivalent resistance in series with C_{ds}

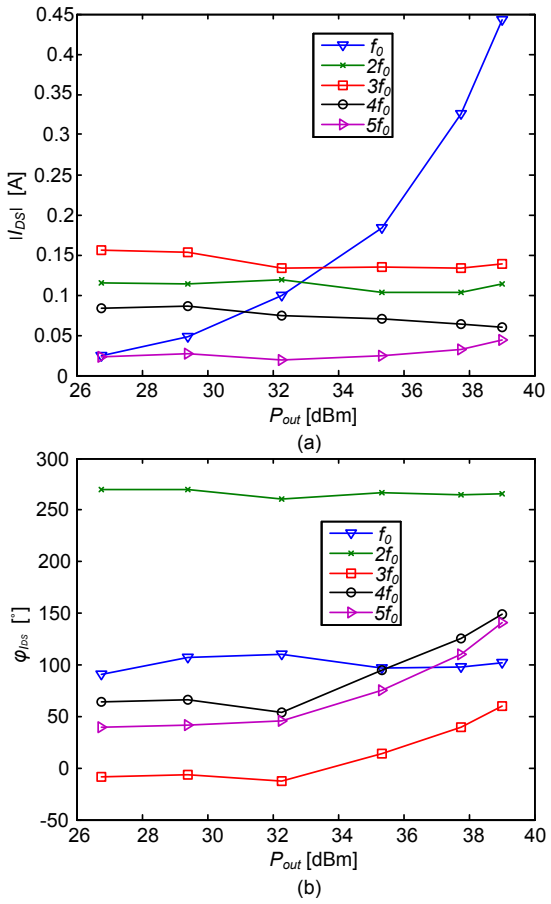

Fig. 4. Harmonic contents of the current waveforms of Fig. 3 in (a) amplitude and (b) phase.

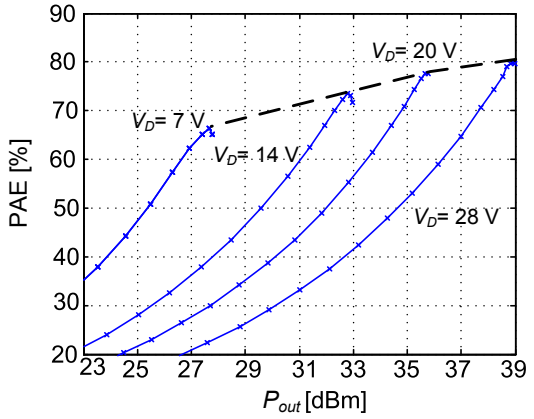

Fig. 5. Power sweep measurements for different V_D values while Z_L is fixed. The dashed line shows the maximum achievable PAE by supply modulation.

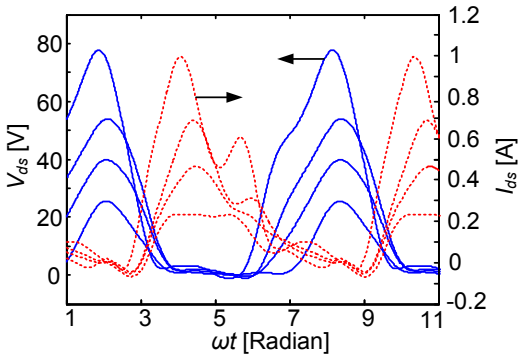

Fig. 6. Intrinsic waveforms of the transistor corresponding to the peak PAE point for each V_D in Fig. 5.

representing technology-dependent parallel losses [9]. γ_2 is a constant coefficient which is dependent on the intrinsic waveform shapes and is not dependant of P_{out}. This equation was presented in [9] as the dominant loss responsible for the efficiency degradations of LDMOS transistors at high drain supply voltages and high frequencies. The equivalent circuit used is, however, general and can be applied for GaN transistors as well.

The shape of the waveforms in Fig. 3 is clearly affected by the load-modulation process. This implies that there is also another source for the PAE degradations in back-off which is related to the fact that the waveforms are no longer optimum compared to the peak power case. For further investigation, the harmonic contents of the output current waveforms in Fig. 3 are extracted and shown in Fig. 4. It is observed that the amplitude of the harmonics are almost constant when the fundamental current decreases by load modulation. This means that the harmonics in back-off are more dominant. There is, therefore, a great potential to take advantage of the dominant harmonic contents to shape the waveforms optimally in back-off where signals having high peak-to-average spend most of the time. For example, the significant variations in the phase of the 4^{th} harmonic, observed in Fig. 4(b), has caused the voltage waveforms to become more flat-top at lower P_{out}. The phase of the 4^{th} harmonic can be optimized for back-off by optimizing the input impedance at the second harmonic.

In the next section, the supply-modulation measurements are presented for the same device to provide a reference of comparison for the results achieved by load modulation.

IV. Supply-Modulation Measurements

Power-sweep measurements for four different V_D's are presented in Fig. 5. The dashed line shows the highest achievable PAE when supply modulation is used. Note that Z_L, $Z_{L,2f_0}$, and $Z_{L,3f_0}$ are the same as optimized for P_{out}=39 dBm in Fig. 2. The intrinsic waveforms, measured and de-embedded to the device current-source reference plane, are shown in Fig. 6 for the peak PAE achieved at each V_D. As shown in this figure, both the intrinsic current and voltage amplitudes decrease when the supply modulation is applied. The dominant loss for the supply modulation is the series loss due to R_{on} [2], [9]. This loss causes the gain to be significantly reduced for this device at lower supply voltages which, in turn, degrades the PAE.

Fig. 7 shows the harmonic contents of the current waveforms in Fig. 6. The amplitude of the harmonics vary only

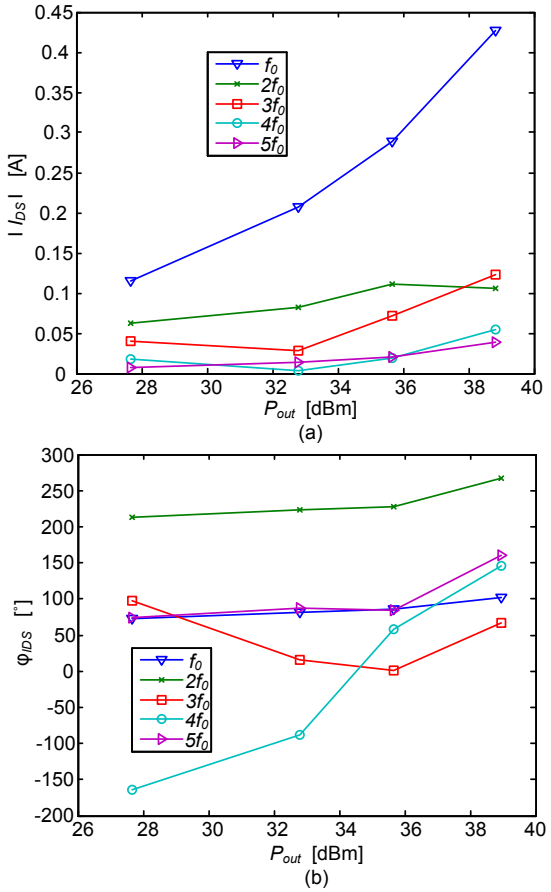

Fig. 7. Harmonic contents of the current waveforms of Fig. 6 in (a) amplitude and (b) phase.

slightly, similar to the case for the load modulation in Fig. 4. However, the phase variation for all harmonics is more significant in the supply-modulation case thus indicating that the waveforms become non-optimal in back-off. The optimization of the harmonic impedances for back-off instead of peak power can help to solve this problem. This is in agreement with the simulation results in [2].

A comparison between the measured results achieved by using either supply modulation or load modulation is presented in Fig. 8. As shown in this figure, both techniques perform almost equally well for the efficiency enhancement at back-off levels $\leq$ 6.5 dB. However, at higher back-off levels, the supply modulation can improve the PAE of the GaN transistor more than the load modulation. This is related to different loss mechanisms involved in each of the techniques.

V. Conclusions

The intrinsic waveforms of a GaN HEMT transistor are extracted from active load-pull measurements and shown to give a detailed insight to the device operation in load- and supply-modulation techniques. It is concluded that there are two main sources for efficiency degradations in both techniques: technology-dependent losses and non-optimal waveforms in back-off. The losses in the load modulation are mainly due

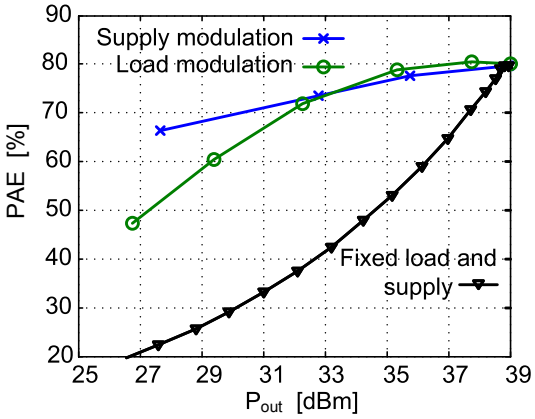

Fig. 8. Comparison between the PAE results achieved for the supply- and load-modulation cases versus P_{out}. The results with fixed load impedance and supply voltage are also included for reference.

to the parallel losses rather than series losses which are dominant in the supply modulation. The problem with non-optimal waveforms in back-off can be solved by circuit-level optimization of harmonic terminations for back-off.

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