APPLICATION NOTE

# CGH40006S, Low Noise Amplifier Demonstrator

## Introduction

Cree has developed a low noise amplifier circuit using a Cree CGH40006S GaN HEMT transistor as a means of demonstrating the wide bandwidth low noise performance and ruggedness of the device. This application note describes the typical performance that has been achieved and that which can be expected when evaluating the demonstrators. Details of the circuit are included for further understanding of the topology and all necessary information has been provided to aid reproduction of the amplifier.

## Features

- Demonstrator of performance over 225 MHz - 2.0 GHz
- 17 dB Small Signal Gain
- >50 % Power Added Efficiency
- <3 dB Noise Figure
- 45 dBm Third Order Intercept
- Intended to be used with C-IED, MilComm, Instrumentation applications


PN: CGH40006S-LNA-KIT

# Basic Amplifier Specification

## Maximum Ratings for Evaluation of Demonstrator at 25°C

| Parameter | Minimum | Maximum | Units | Notes |
|---|---|---|---|---|
| Gate-to-Source Voltage | -10 | +2 | Volts | |
| Frequency | 0.225 | 2 | GHz | |
| Input Power Level | - | 39 | dBm | CW No Degradation |
| Input Power Level | - | 42 | dBm | CW Device Failure |
| Input Power Level | - | 44 | dBm | Pulsed 300µs 10% Duty Cycle No Degradation |
| Input Power Level | - | 46 | dBm | Pulsed 300µs 10% Duty Cycle Device Failure |
| Operating Junction Temperature | - | 175 | °C | |
| Case Temperature | -40 | +150 | °C | |

## Summary of Typical Low Noise Amplifier Demonstrator Performance

| Characteristics | Frequency | | | | Units |
|---|---|---|---|---|---|
| | 225 MHz | 500 MHz | 1000 MHz | 2000 MHz | |
| Small Signal Gain | 18.5 | 18.0 | 17.0 | 17.5 | dB |
| Input Return Loss | -12.5 | -9 | -7 | -6 | dB |
| Power Gain $P_{IN}$ =25 dBm | 13.7 | 13.5 | 13.2 | 12.8 | dB |
| Power Added Efficiency $P_{IN}$ = 25 dBm | 57.5 | 57.0 | 50.0 | 40.0 | % |
| Noise Figure | 1.75 | 2.1 | 2.5 | 3.15 | dB |

Note 1: $I_{DQ}$ = 50 mA

Note 2: Individual device characteristics are as per CGH40006S data sheet

Note 3: $V_{GS}$ has been selected for best noise figure / efficiency tradeoff

## Typical Circuit Bias Conditions

| Circuit Element | Bias Voltage | Quiescent Bias Circuit |
|---|---|---|
| Gate Bias | -3.0 | 50 mA |
| Drain Voltage | +28 | NOTE: GATE BIAS MUST BE APPLIED BEFORE THE DRAIN BIAS IS ACTIVATED. |



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## Details of the CGH40006S Demonstrator Circuit

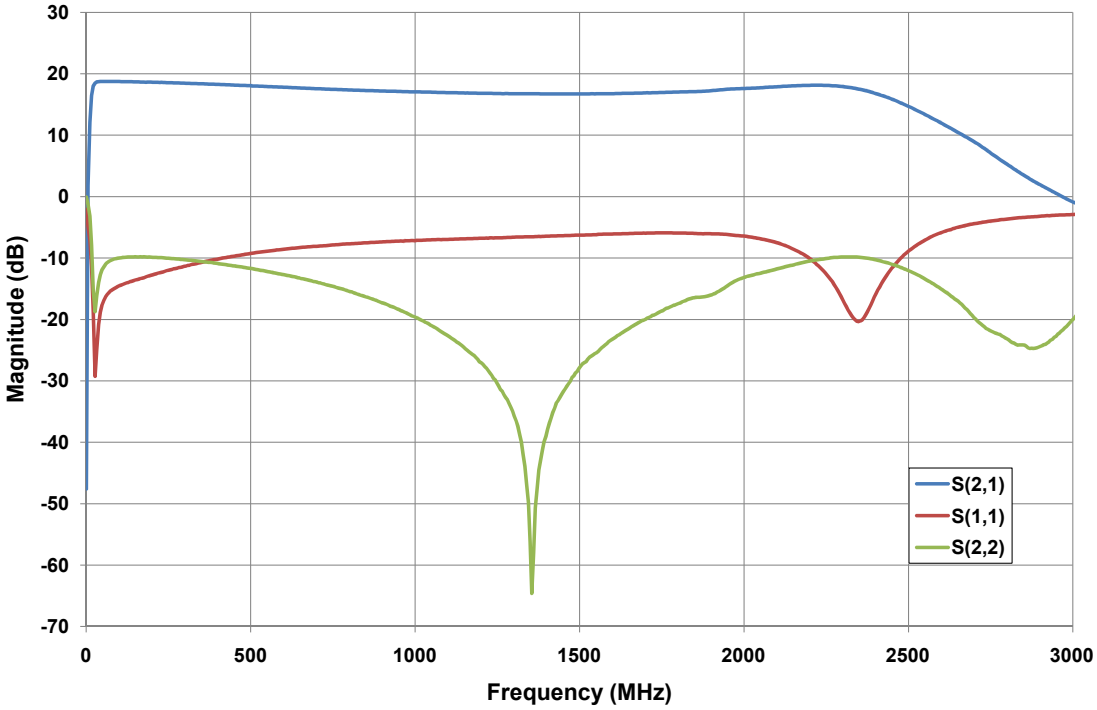


Figure 1 -CGH40006S LNA Circuit Typical S-parameters
$V_{DD}$ = 28 V, $I_{DQ}$ = 50 mA

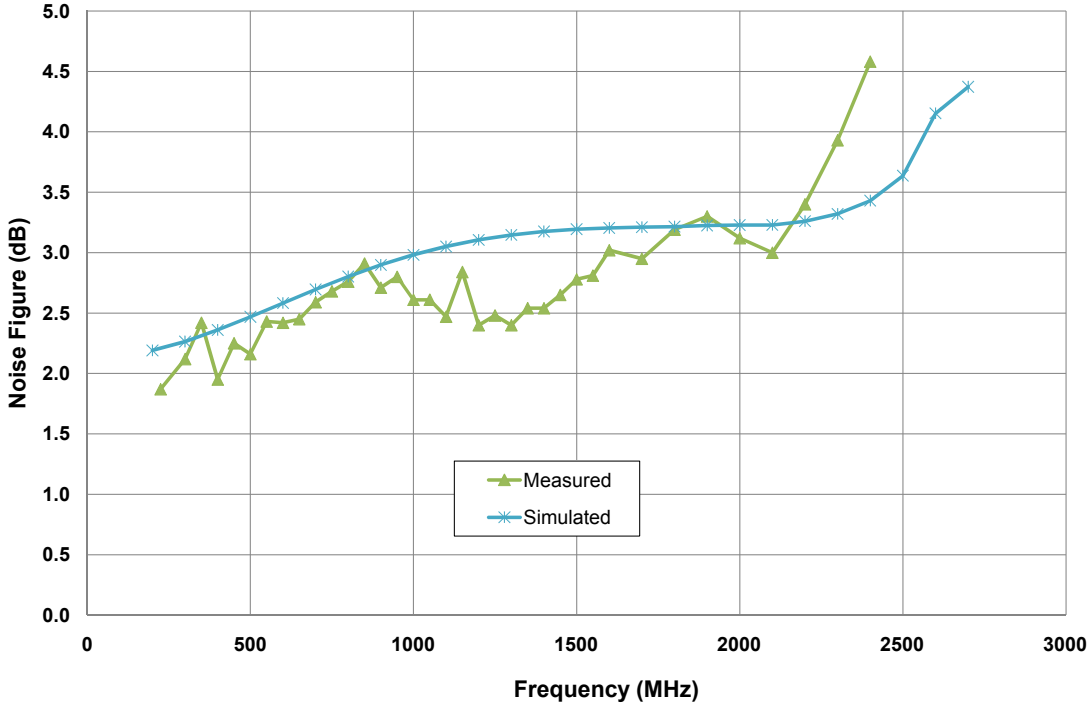


Figure 2 -CGH40006S LNA Noise Figure vs Frequency



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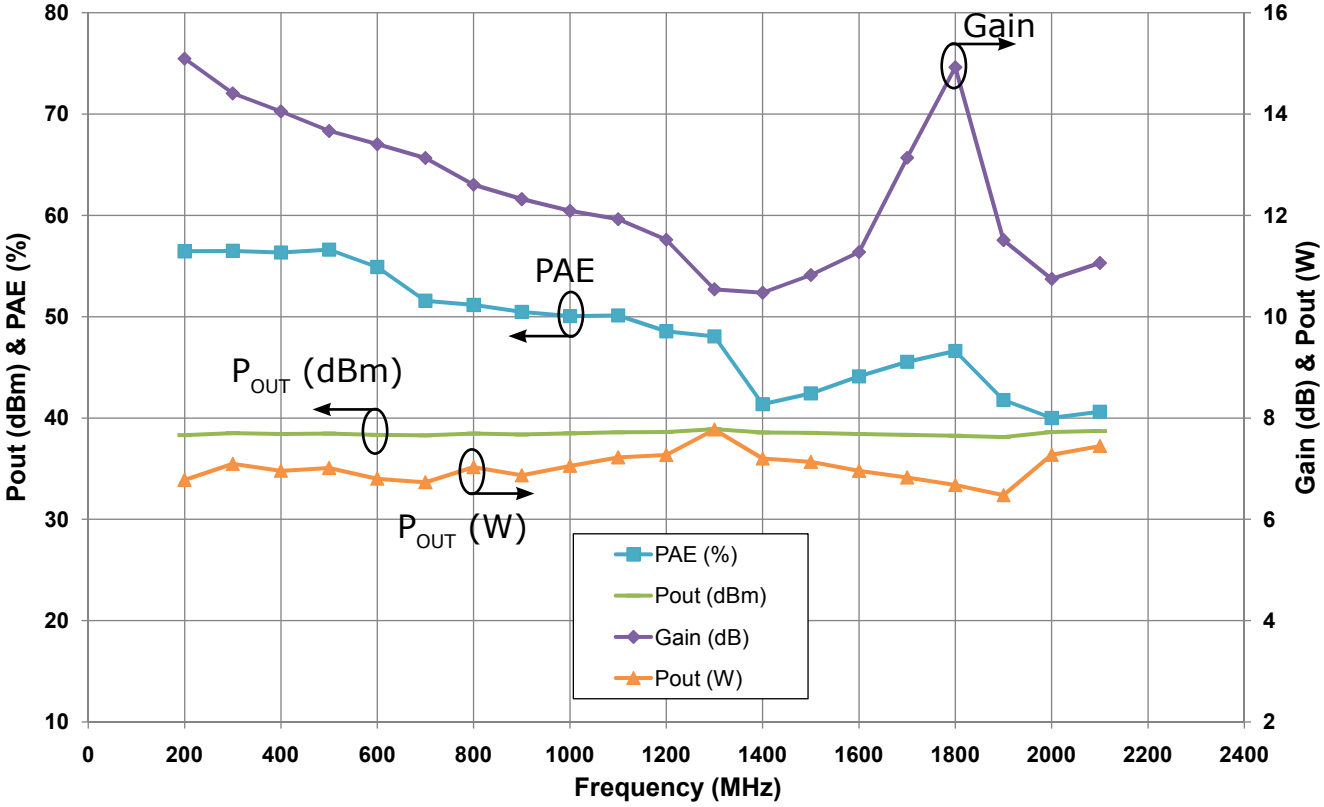


Figure 3 -CGH40006S LNA Circuit
$P_{SAT}$, PAE and Power Gain vs Frequency



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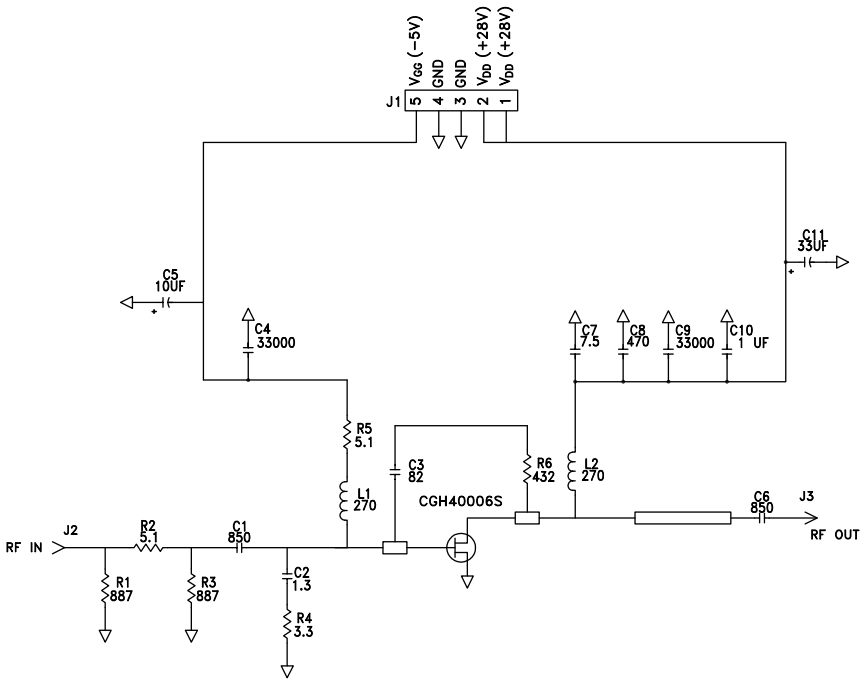


Figure 4 - Schematic of CGH40006S-LNA-KIT Demonstrator Circuit

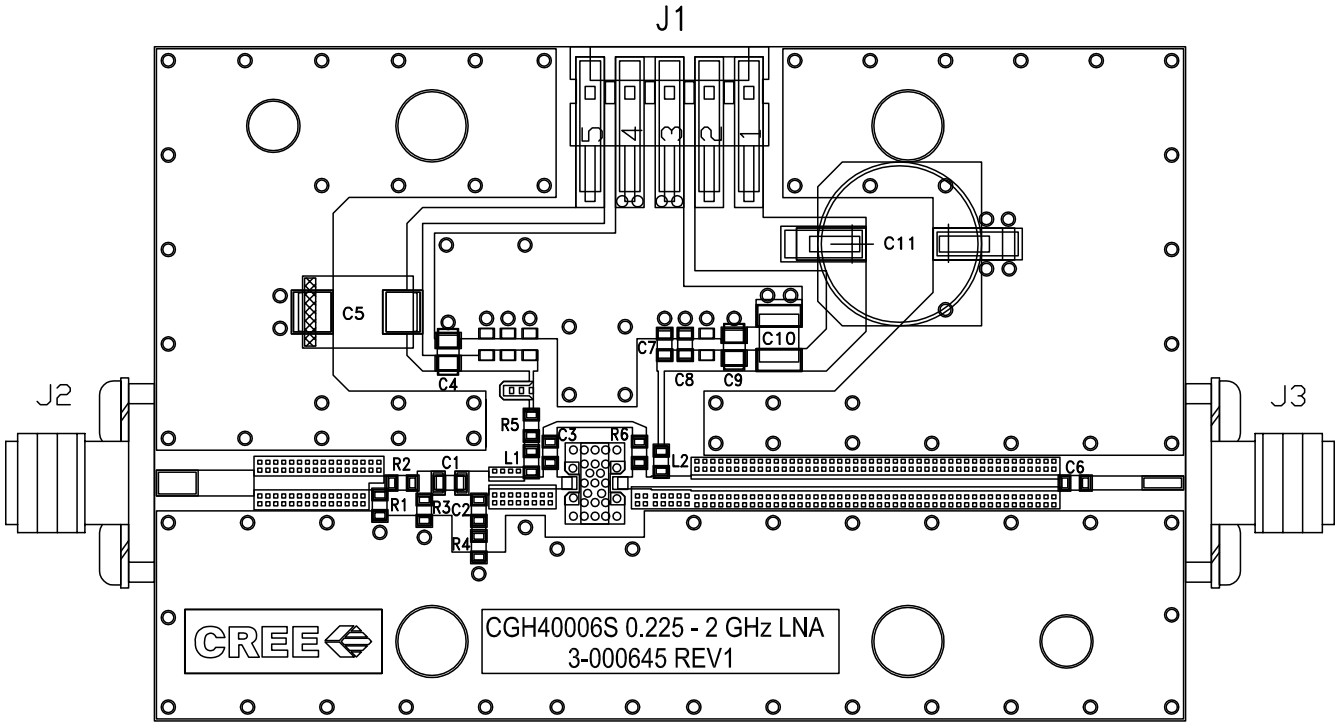


Figure 5 - CGH40006S-LNA-KIT Demonstrator Printed Circuit Board Assembly



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## Details of the CGH40006S LNA Demonstrator Circuit continued

### CGH40006S Demonstrator Bill of Materials

| Reference Designator | Description | Quantity |
|---|---|---|
| R1, R3 | RES, 1/16W, 0603, 1%, 887 Ohms | 2 |
| R2, R5 | RES, 1/16W, 0603, 1%, 5.1 Ohms | 2 |
| R4 | RES, 1/16W, 0603, 1%, 3.3 Ohms | 1 |
| R6 | RES, 1/16W, 0603, 1%, 432 Ohms | 1 |
| C1, C6 | CAP, DC BLOCK, MULTI-LAYER, 0603, 850pF | 2 |
| C2 | CAP, 1.3pF, +/-0.1pF, 0603, ATC | 1 |
| C3 | CAP, 82.0pF, +/-5%, 0603, ATC | 1 |
| C5 | CAP 10uF, 16V, TANTALUM | 1 |
| C7 | CAP, 7.5pF, +/-0.1pF, 0603, ATC | 1 |
| C8 | CAP, 470pF, 5%, 100V, 0603 | 1 |
| C9 | CAP, 33000pF, 0805, 100V, X7R | 1 |
| C10 | CAP, 1.0uF, 100V, 10%, X7R, 1210 | 1 |
| C11 | CAP, 33 uF, 20%, G CASE | 1 |
| L1,L2 | INDUCTOR, SMT, 0603, 270nH, 5%, RoHS COMPLIANT | 2 |
| J1 | HEADER RT>PLZ .1CEN LK 5POS | 1 |
| J2,J3 | CONN, SMA, PANEL MOUNT JACK, FLANGE, 4-HOLE, BLUNT POST | 2 |
| | PCB, RO4350B, 20 MIL THK, CGH40006S 225 MHz - 2 GHz LNA APPLICATION CIRCUIT | 1 |
| | 2-56 SOC HD SCREW 1/4 SS | 4 |
| | #2 SPLIT LOCKWASHER SS | 4 |

## Conclusion

This application note has shown the performance advantages of using discrete GaN HEMT transistors for low noise amplifiers. The reference design here shows that it is possible to achieve wide bandwidths, high power and efficiency whilst maintaining low noise and is able to withstand CW input power of 5 W with no degradation. As this transistor is unmatched performance can be replicated at other frequency bands. This reference design was generated with first pass success using Cree's large signal models, which are available on request.



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## Cree CGH40006S Low Noise Amplifier Demonstrator Setup Instructions

1. Position the demonstrator amplifier fixture such that the RF source (50Ω) is connected to the left side of the fixture and the RF load (50Ω) is connected to right side of the fixture.

2. Connect the 5-pin bias cable.

3. Verify all power supplies are at 0 volts before turning on.

4. Connect the test fixture **RED** wires to the drain power supply.

5. Connect the test fixture **WHITE** wire to the gate power supply.

6. Connect the test fixture **BLACK** wires to the return (common) terminals of the gate and drain power supplies.

7. Verify connections with the schematic shown in Figure 4.

8. Turn on the gate bias power supply. Adjust the power supply to -5.0 V.

9. Turn on the drain bias power supply. Adjust the power supply to +28 Volts. There should be NO current flow from the power supply.

10. Adjust the current by changing the gate bias supply for a drain current (Idq) of 50mA.

11. Apply low RF drive, 10 dBm (1000 MHz), and verify the fixture has approximately 17 dB of gain. Increase RF drive to the desired output level and verify the performance with the transistor data sheet.

12. To shut down the circuit: Turn off the RF test signal. Turn off the +28 V Drain supplies and lastly turn off the gate voltage supplies.



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