

A Linear and Efficient Doherty PA at 3.5 GHz

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This article outlines the design procedure and presents the results of the winning power amplifier (PA) design at the PA competition held at the 2012 IEEE MTT-S International Microwave Symposium (IMS2012) and sponsored by the High-Power Microwave Components Committee (MTT-5). Traditionally, the figure of merit (FOM) employed was the maximum continuous wave (CW) power added efficiency (PAE) multiplied by a frequency weighting factor

$$\text{FOM} = \frac{P_{\text{RF,out}} - P_{\text{RF,in}}}{P_{\text{DC}}} \cdot \sqrt[4]{f_c}$$

However, this time, a major modification has been introduced to the PAE measurement: aiming to reflect linearity as well, the PAE is to be measured when producing a two-tone carrier-to-intermodulation ratio (C/I) of 30 dB [1]. In the following, it will be explained how this has seriously affected the strategy behind the

choice of the PA architecture. Unlike earlier single-track PA designs, a Doherty with driver stage design was made (see Figure 1), employing Cree's CGH40006P GaN HEMT [2]. For a 30 dBc C/I, the circuit delivered 6.5 W average output power with a two-tone PAE of 59% (66% two-tone drain efficiency) at 3.5 GHz.

Concept and Motivation

Circuit design should always start with a careful analysis of the specification to be fulfilled. From a mathematical point of view, the FOM shows a hyperbolic dependence on frequency. This means that the benefit due to increasing the frequency declines at higher frequencies. From a technical point of view, the selection of the optimum design frequency constitutes a trade off between the offered boost in FOM and the potential to achieve high efficiency at this frequency, which is limited by the available device technology.

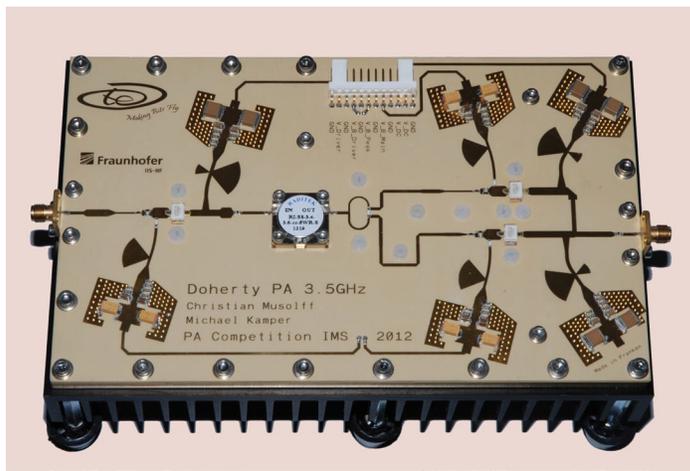


Figure 1. A picture of the fabricated doherty PA.

Since linearity became a main criterion in the competition, a two-tone excitation is used in order to assess the IMD along with the PAE.

For a solid-state design with commercially available GaN HEMTs, a good trade off is in the range of 3–4 GHz. We chose 3.5 GHz as a center frequency; this frequency is used commercially in WiMax applications, and suitable components are broadly available.

To be considered next are the conditions under which the PAE is measured. Since linearity became a main criterion in the competition, a two-tone excitation is used in order to assess the intermodulation distortion (IMD) along with the PAE. The two-tone signal, however, doesn't have a constant envelope but resembles an AM signal with suppressed carrier, modulated

by a beat tone, whose frequency equals half the tone spacing. Consequently, it results in a 3 dB peak to average power ratio (PAR). The two-tone PAE therefore not only depends on the amplifier's peak efficiency, but also on its efficiency in backoff. Since that is a very common problem in linear amplifiers typically operated to amplify modulated signals with high PAR, many techniques to improve back-off efficiency have evolved. They either rely on supply voltage modulation or on a modulation of the load. Doherty architecture (see Figure 2), being the most prominent technique to implement active load modulation, was selected for this project. It consists of two active devices whose outputs are connected by a certain type of combiner featuring an impedance inversion property and allowing the active devices to maintain high-efficiency operation even in backoff (see Figure 3).

For a two-tone excitation, it provides more than 11% higher average efficiency when compared to a normal class B amplifier.

The basic principles of the Doherty amplifier itself, however, won't be discussed within this article. Readers who are not familiar with the matter are kindly referred to [3] and [4].

Another important aspect extracted from the competition rules is related to the gain of the amplifier. The rules specify a maximum input power of 18 dBm and a minimum required output power of 2.5 W (≈ 34 dBm), resulting in a gain of at least 16 dB. This is quite critical, as it is close to the limits of what can be achieved with a single-stage amplifier at the chosen frequency of 3.5 GHz. The gain of a Doherty amplifier is usually even lower than that of a single-path PA. Biased in class C, the peak path of a Doherty amplifier has inherently lower gain. Also, the input distribution circuit of a Doherty amplifier implicates some additional losses

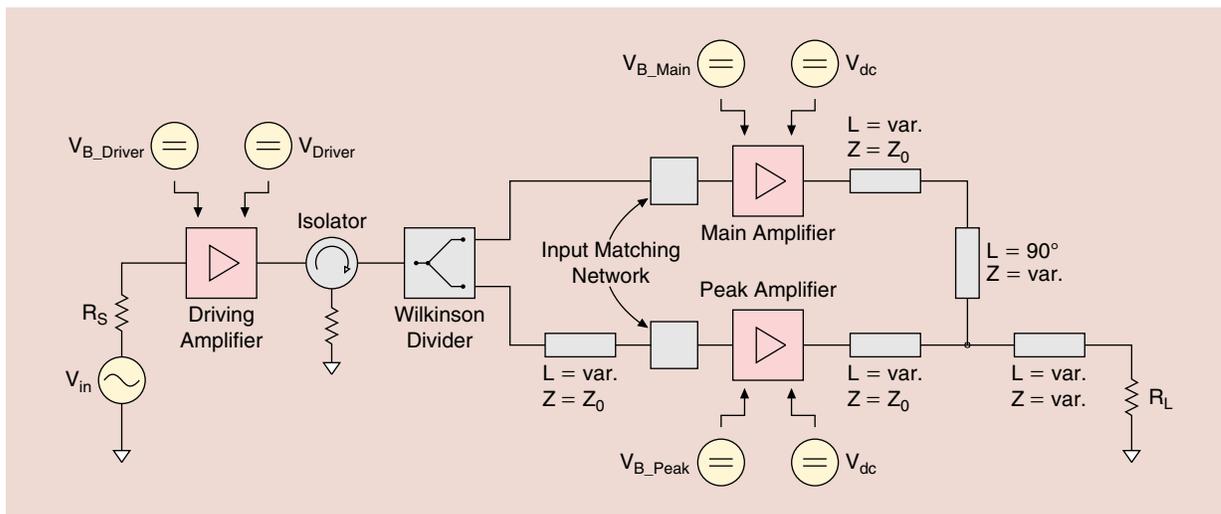


Figure 2. A block diagram of the Doherty PA with driver stage.

Two-tone harmonic balance simulation in Agilent Advanced Design System [5] is applied to design and optimize the amplifier.

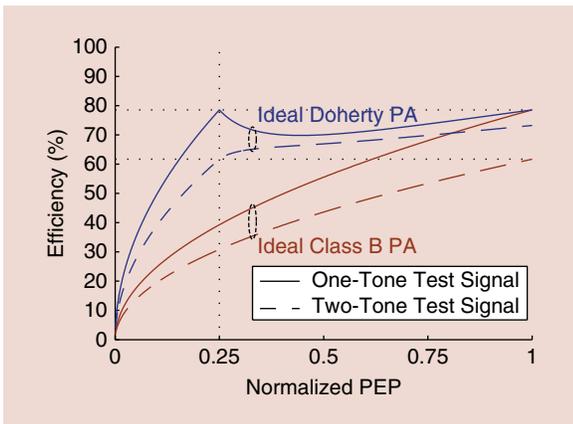


Figure 3. Efficiency for ideal single-path PA and ideal Doherty for one-tone and two-tone excitation.

and therefore reduces the overall gain. It is almost impossible to achieve 16 dB of gain in a Doherty amplifier at 3.5 GHz with the active devices that we use. This makes the inclusion of a driver stage mandatory.

Incorporating a driver stage brings in yet another problem. In order to achieve good efficiency, the driver stage is biased in class AB. Thus, its output impedance varies with output power and doesn't constitute a good match to the input of the Doherty amplifier. This is unacceptable, as it deteriorates the isolation and input matching of the main and peak paths, subsequently undermining the performance of the Doherty amplifier. As an effective workaround, an isolator is inserted between the driver stage and the Doherty amplifier.

Facing time pressure, we set our most important task to finding a first-pass design methodology. A

simulation-based design is the only way to achieve optimal results with just one iteration. Assuming that the simulator is properly set up, the success of this method solely depends on the accuracy of the modeling. With a 2.5 dimensions simulator like Momentum [5], the electromagnetic (EM) modeling of microstrip circuits is quite accurate and yet effective. Therefore, we mostly relied on microstrip implementations of passive subcircuits and tried to avoid lumped surface mount technology (SMT) components, which are more difficult to model accurately.

Besides a reliable design of passive subcircuits, the most crucial point in simulation-based PA design is modeling of the active devices. In this context, a decisive argument for adopting Cree's GaN HEMTs is the availability of large signal models, which are well established and reasonably accurate.

Simulation

Two-tone harmonic balance (HB) simulation in Agilent Advanced Design System (ADS) [5] is applied to design and optimize the amplifier. In the first step, a very basic simulation environment is set up, in which ideal representations of all passive subnetworks are used. Input matching and harmonic tuning are

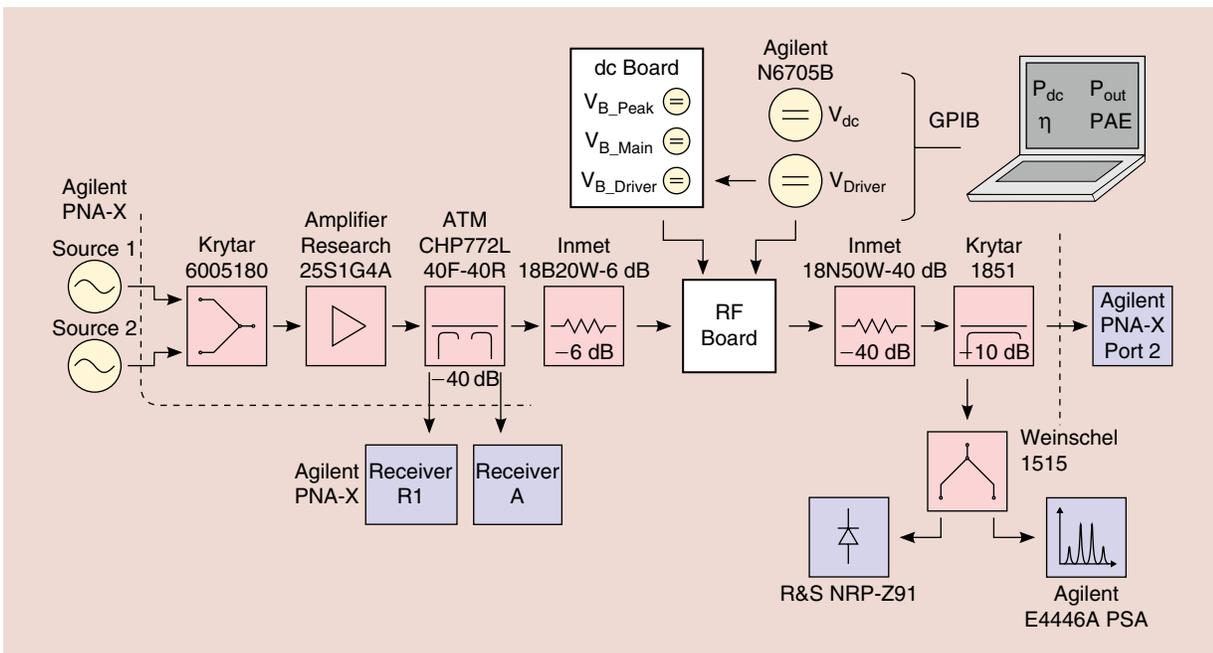


Figure 4. An overview of the high-power measurement setup.

The first finding from the simulation was that a careful design of the second harmonic termination is mandatory as it offers a considerable increase in efficiency.

realized as equation-based linear two ports (S2P_Eqn). The Doherty combiner can, at least in a narrowband situation, be represented by four ideal transmission lines (TLIN). The lengths of three and the impedances of two of them map to the five degrees of freedom that the Doherty combiner offers (see Figure 2).

An important point is also to consider the terminations at baseband (strictly speaking, at all frequency points that are used by HB). Leaving these terminations

unattended (e.g., just using an ideal dc feed, which is an open circuit at baseband) will produce wrong simulation results or convergence problems.

After setting up the simulation environment, a simulated load-pull measurement, including second and third harmonics, is done to find the optimum output terminations. Likewise, the optimum source matches are found. By using two-tone HB, linearity can also be evaluated in this process. The first finding from the simulation was that a careful design of the second harmonic termination is mandatory as it offers a considerable increase in efficiency. This matches our expectations, because bias points between deep class AB and class C are used, which should result in a large content of even harmonics in the drain current.

The termination of the third harmonic can be neglected since the amplifier is required to operate in a very linear region, where third harmonic power available at the drain is too low to justify the complexity of a distinct termination.

With the help of the load-pull data, a rough layout of the Doherty combiner can be done, using common Doherty design methodology [4]. This initial solution is then used as a starting point for optimization, based on a two-tone HB simulation with swept input power to further improve the design.

Owing to the high number of variables (16) to be optimized, a sequenced optimization is used, which iteratively improves different combinations of optimization variables and error functions. The error functions are composed of third- and fifth-order intermodulation ratio, output power, PAE, and input voltage standing wave ratio (VSWR). In order to find a robust and well-centered solution and to avoid running into deceptive, narrowband solutions, a few swept error variables are introduced. They are added to critical optimization variables and swept between three values in the range of a few percent. For the same reason, the center frequency is also swept over three points in a

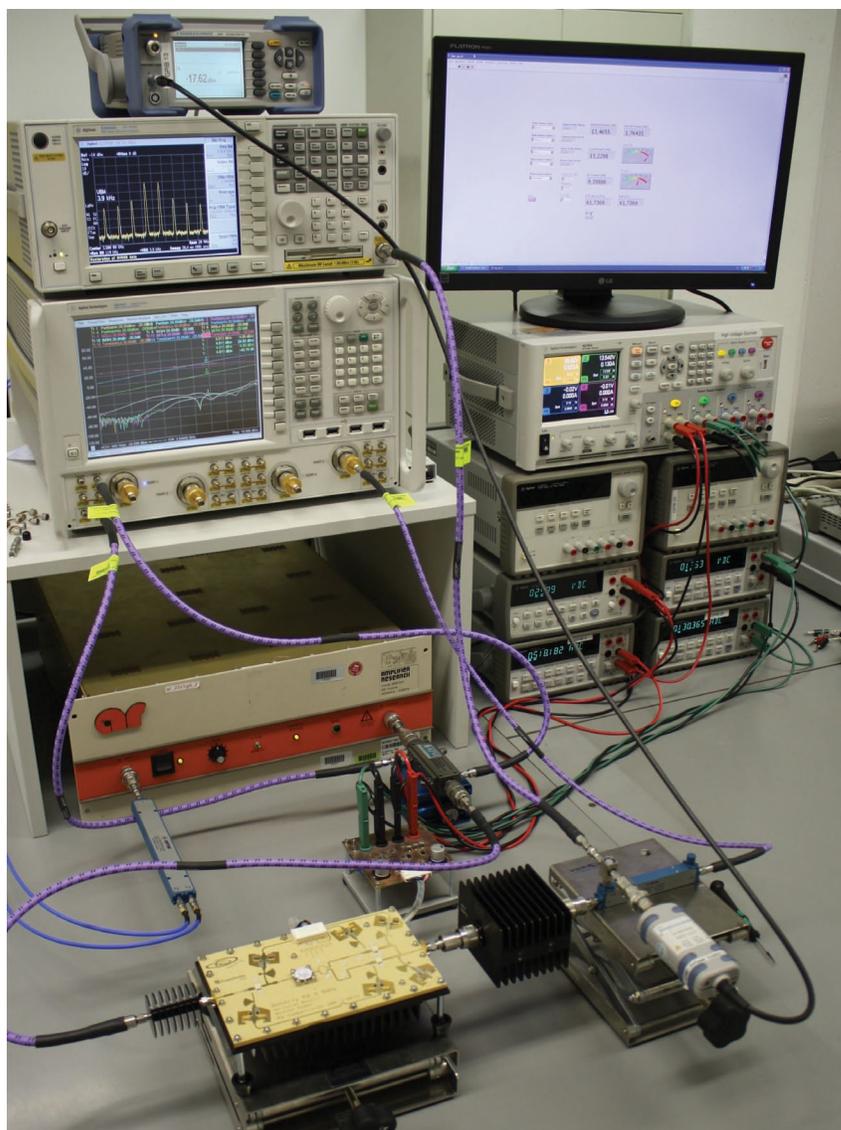


Figure 5. Doherty PA at the test bench.

range of 50 MHz. This results in a multidimensional sweep and increases simulation time, but it is still less time-consuming than purely statistical design methods like yield optimization or Monte Carlo.

Having found an optimized and robust solution for the input matching and the Doherty combiner (including second-harmonic termination), we begin the actual realization of the passive subnetworks with the design of the input networks.

To analyze small signal stability in the relevant frequency range (10 MHz–10 GHz), S-Parameters at different bias conditions are extracted from the transistor model and cascaded with the input network. Stabilization measures in the input network can then be designed using classical small-signal stability analysis (i.e., stability circles and geometrically derived stability parameters [6]). By adding an S-probe, the reflection coefficient presented to the gate can be observed and insertion loss at passband can be calculated.

The input networks are designed using mostly microstrip circuit models (MLIN). Lumped components are initially assumed to be ideal and later replaced by more realistic SMT component models. To achieve a reasonable stabilization at low frequencies, a shunt resistor (50 Ω) is added to the bias line as well as a resistor-capacitor (RC) (50 Ω || 1.8 pF) network in series to the input. This, in connection with the shunt capacitance imposed by the rather wide microstrip line at the gate terminal, provides a good stabilization over the entire frequency range. The insertion loss of the network at passband is around 0.6 dB.

After completing the circuit design for the input network, EM simulation is applied. It turns out that the stabilization properties of the network are still satisfying and only minor changes are to be made. To account for small changes in the reflection coefficient at passband, the parameterized EM model is reoptimized manually, based on a few parameter sweeps.

The final input networks, represented by EM component models, are then included into the HB simulation, and the whole setup is optimized again to account for (marginal) differences between the ideal network and the final EM model.

The procedure for realizing the Doherty combiner is essentially the same as with the input matching networks, a circuit model is designed and optimized to fit the ideal representation as well as possible, and then a parameterized EM model is created from it and retuned manually.

To complete the design of the Doherty PA, the input distribution network is realized, again using the same design flow. It comprises a slightly asymmetric Wilkinson divider and a delay line for the peak amplifier. A further requirement for this network is to com-

The process temperature of 230 °C poses only a low thermal stress on the components.

pensate for geometric differences in the layout of the main and peak paths so that, in the end, everything fits together neatly.

The driver stage is implemented as a class AB amplifier based on the already existing simulation environment and design flow. Input and output matches are optimized for deep class AB operation at about 27 dBm output power, good linearity and adequate efficiency. For convenience, the same active device as in the Doherty PA is used but at a drain bias of only 13.5 V, due to the much lower output power level that is needed.

Finally, a two-tone HB simulation of the whole amplifier, including driver, is performed in order to assess the linearity and PAE of the whole chain. Simulation results are very promising. The predicted PAE at an IMD of –30 dBc is around 64% and the IMD in backoff always stays below –34 dBc. The influence of a possible mismatch of the isolator is also analyzed; for a maximum VSWR of 1.2, as specified by the manufacturer, the results are still acceptable. The same holds true for slight mismatches of the amplifier's source and load terminations.

Manufacturing

Having placed so much effort into modeling and simulation of the amplifier, we wanted to make sure that additional inaccuracies due to manufacturing are kept as low as possible by using high-quality components, materials, and manufacturing techniques.

Rogers TMM3 laminate with an ϵ_r of 3.39 and a thickness of 20 mil is chosen for the design of the RF board [7]. Its low $\tan\delta$ and high thermal and mechanical stability make it a good choice for PA design. The dielectric constant and substrate thickness are selected according to the 3.5 GHz center frequency, keeping copper losses and manufacturing tolerances in good balance.

The RF transistors come in pill packages that have to be soldered directly to a solid backplane. This 6-mm-thick backplane is a brass plate. A galvanic gold plating ensures a good soldering surface as well as long-term stability. High-quality subminiature version A (SMA) flange connectors are directly mounted to the ends of the backplane.

A vapor-phase soldering technique is applied in order to guarantee good soldering of the transistors and passive flip-chip components. The process temperature of 230 °C poses only a low thermal stress on the components. The assembled module is tempered to

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150 °C before soldering, taking the high thermal capacity of the backplane into account.

Measurement Setup

A block diagram of the measurement setup is shown in Figure 4. Figure 5 shows a photograph of this setup.

The competition rules allow a maximum of two dc sources. Those are used to supply drain bias to the Doherty stage (26 V) and the driver stage (13.5 V), respectively. Auxiliary voltages needed to bias the transistors' gates are generated from the drain bias of the driver stage on a dedicated dc board. For this purpose, the positive supply voltage is inverted by a low-power charge pump and the respective gate voltages are then stabilized by three linear regulators. All losses generated in the dc board (≈ 20 mW) are included in the PAE measurement.

A two-tone test signal is generated by combining the two sources of the PNA-X network analyzer in an external combiner. The signal is then preamplified and supplied to the device under test (DUT). A directional coupler at the output of the preamplifier is used to measure and calibrate the input power. Source impedance uncertainties at the test port are reduced by an additional 6 dB attenuator. The output of the DUT is directly connected to a 40 dB attenuator and then supplied to the second port of the network analyzer for measurement of IMD and output power. A 10-dB directional coupler diverts a part of the signal to a power meter and a spectrum analyzer for a comparative measurement of power and IMD. The instruments are connected to a PC via general purpose interface bus (GPIB) and Ethernet, where a Labview program calculates dc powers and efficiencies.

Even slight measurement errors can significantly distort the efficiency reading. Therefore, an accurate calibration of the setup is required. Using an external power sensor, first the port 1 reference receiver of the PNA-X network analyzer is calibrated for absolute power measurement. Subsequently, a through standard is used to transfer the power calibration to the port 2 test receiver. The used power sensor is specified with an uncertainty for absolute power measurements of 0.06 dB at 3.5 GHz. This corresponds to an uncertainty of 1.4% in the efficiency measurement. Additional errors in the calibration due to mismatch are present, but mitigated by the attenuators, which create a well-matched environment at the test ports. The uncertainty for dc power is less than 0.1%. Overall, a measurement uncertainty of 0.1 dB in absolute power and 2.5% in efficiency is a realistic estimate.

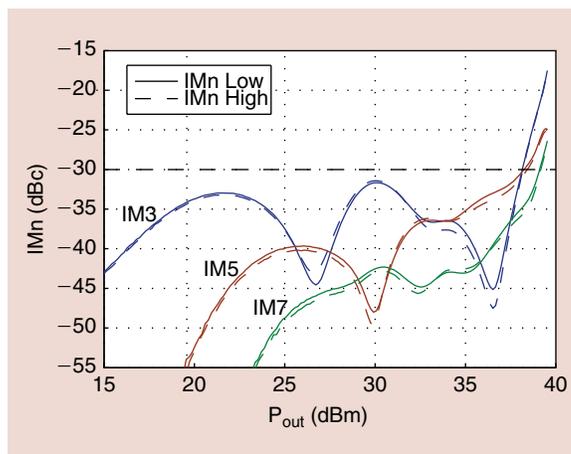


Figure 6. Measured n th-order intermodulation (IM_n) versus output power: the IM_3 stays below 30 dBc up to a point of abrupt compression.

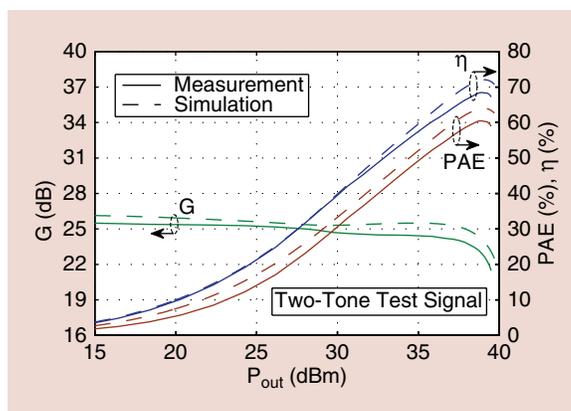


Figure 7. The drain efficiency, PAE, and gain versus output power for a two-tone test signal at 3.5 GHz.

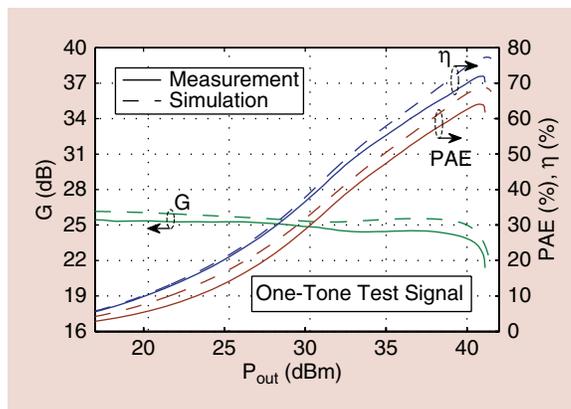


Figure 8. The drain efficiency, PAE, and gain versus output power for a one-tone test signal at 3.5 GHz.

The results of the comparative measurement that was done with a power meter and spectrum analyzer also stayed well inside this range.

A careful selection of power levels and attenuation is necessary to maximize the dynamic range of the setup [8]. The preamplifier is leveled well in backoff, where its IMD is negligible. To avoid nonlinear effects in the PNA-X receivers, the maximum power at their inputs should not exceed -20 dBm.

With an input power sweep range of 30 dB and a measurement bandwidth of 50 Hz, intermodulation products can be measured accurately down to -50 dBc even at the lowest input power level.

Memory effects in the DUT are noticed at higher powers. To verify the amplifier in true CW operation and comply with the conditions of the competition, a high dwell time (20 s) is used so that measurements are recorded only after a stable state has been reached. This can be regarded as a worst case scenario.

Results

The amplifier maintains a high level of linearity over the entire range of output power. By exploitation of cancellation effects, third-order intermodulation is mitigated up to a point of abrupt compression, which can be seen in Figure 6. Linearity sweet spots are a common phenomenon even in traditional class AB PAs. In a Doherty PA however, such cancellation effects become more prominent and more than one sweet spot can occur, due to the interaction of main and peak amplifier, which have different bias points and thus different transfer characteristics. In our design, these effects were explicitly included in the optimization of bias points and the Doherty combiner.

At the upper edge of the linear range, a drain efficiency of 70% is reached, which is outstanding (see Figure 8). Even though its backoff efficiency characteristic doesn't resemble an ideal Doherty amplifier (which was neither intended nor even possible, taking into account the high linearity and restriction to classical single-input drive), the improvement due to load modulation is clearly visible in Figure 8. In terms of two-tone efficiency with a C/I of 30 dBc, the improvement compared to a regular class AB amplifier with the same active device is higher than 10% (see Figure 7).

A good match between simulation and measurement was achieved with regard to drain efficiency. Even the prediction of linearity was acceptable. This demonstrates the feasibility of simulation-based design of Doherty PAs, despite the challenging problem of active load modulation. Unfortunately, there is a significant discrepancy between simulated and measured PAE. This can be traced back to inaccuracies in the simulation of the driver. A considerably higher quiescent current than in simulation had to be used in order to achieve acceptable performance of the driver stage. It turns out that the transistor model's accuracy is degraded due to the low drain voltage of only 13.5 V, which is well below the specified range.

In terms of two-tone efficiency with a C/I of 30 dBc, the improvement compared to a regular class AB amplifier with the same active device is higher than 10%.

Conclusion

In this work, a very good match between simulations and measurements of a Doherty PA was observed. To the best of authors' knowledge, the achieved results demonstrated the highest performance in terms of two-tone efficiency at high linearity that can be found in literature. With this simulation-based design, the possibility of successfully achieving a desired performance in practice, even in terms of linearity, has been demonstrated for a multipath PA architecture. That was possible due to the thorough design procedure followed, with special attention to robustness of the design and critically due to the availability of accurate transistor models, which are ultimately needed for next-generation PA designs (e.g., load modulated architectures).

Acknowledgments

We would like to conclude this article with a few words of acknowledgment to the people who supported our work: Fraunhofer IIS, Erlangen, for providing the infrastructure that allowed us a precise mechanical realization of the hardware; Nokia Siemens Networks, Ulm, and the ESI Application Center (Embedded Systems Initiative) for the funding of PA-related research at our institute; Mathias Otto from Tactron Electronics for supplying critical components on short notice, and, last but not least, Cree Inc., for providing the active device models and samples.

References

- [1] Announcement of the student competition. (2012). [Online]. Available: http://ims2012.mtt.org/files/IMS2012_HEPA_NewRules%20doc.pdf
- [2] *CGH40006 6W, RF Power GaN HEMT*. Durham, NC: Cree Inc., Apr. 2012.
- [3] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," *Proc. IRE*, vol. 24, no. 9, pp. 1163–1182, Sept. 1936.
- [4] S. C. Cripps, *Advanced Techniques in RF Power Amplifier Design*. Norwood, MA: Artech House, 2002.
- [5] Agilent Technologies. (2011). Advanced Design System (ADS) 2011.10 with Momentum planar EM simulator, Santa Clara, CA. [Online]. Available: <http://www.agilent.com>
- [6] M. L. Edwards and J. H. Sinsky, "A single stability parameter for linear 2-port circuits," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1992, vol. 2, pp. 885–888.
- [7] Rogers Corp. (2010). TMM Thermoset Microwave Materials. [Online]. Available: www.rogerscorp.com
- [8] Agilent Technologies. (2011). Optimizing Dynamic Range for Distortion Measurements. [Online]. Available: www.agilent.com

