Advanced Design of a Double Doherty Power Amplifier with a Flat Efficiency Range

Yong-Sub Lee, Mun-Woo Lee, Sang-Ho Kam, and Yoon-Ha Jeong

Department of Electronic and Electrical Engineering, Pohang University of Science and Technology, Pohang, Gyungbuk, 790-784, Republic of Korea

***Abstract* — This paper reports a new double Doherty power amplifier (DDPA) with a flat efficiency range, which consists of two-stage amplifiers. When the two-way DPA is used as the main peaking amplifier, the driving peaking cell with class-C bias turns the DPA off before the saturation of the main carrier amplifier. Three efficiency-peaking points are achieved with the additional Doherty operation by the main peaking amplifier after the saturation of the main carrier amplifier. For verifications, the driving and main amplifiers are designed and implemented with 2-W and 10-W GaN HEMTs, respectively, at 2.14 GHz. From the continuous wave (CW) results, three efficiency-peaking points are obtained at approximately 9-, 5-, and 0-dB back-off powers with over 42% drain efficiency. For one-carrier wide-band code division multiple access (WCDMA) signal, the DDPA shows good digital predistortion linearization performance.**

***Index Terms* — Doherty amplifier, efficiency, linearization, power amplifier.**

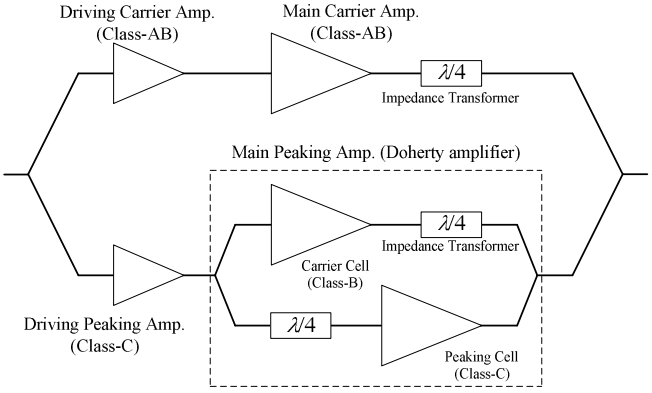

Fig. 1. Schematic diagram of the proposed DDPA.

I. Introduction

Doherty power amplifiers (DPAs) have been widely investigated and developed as the prime candidate for high efficiency at a large back-off power (BOP) [1]-[9]. Recently, modulated signals in the modern communication systems have a high peak-to-average power ratio (PAPR) of over 9 dB. Thus, various extended DPAs, such as *N*-way or multi-stage Doherty structure, asymmetrical DPA using uneven device ratio, and so on [2]-[8], have reported to obtain high efficiency at a large BOP since the conventional DPA shows the peak efficiency at a 6-dB BOP. However, these extended DPAs have one of serious drawbacks as shown below.

1) Low power gain by *N*-way input power divider, which lays a burden on the drive amplifier.
2) Significant efficiency drop between two efficiency-peaking points.
3) Different device matching and delay mismatch due to uneven device ratio or saturation power.

In order to solve these problems, we propose a new double DPA (DDPA) with a flat efficiency range. By employing the two-way DPA as the main peaking amplifier, three efficiency-peaking points can be achieved by double Doherty operation since the Doherty operation of the main peaking amplifier is obtained after the saturation of the main carrier amplifier. The driving peaking amplifier with class-C bias keeps the carrier cell of the DPA turning off before the saturation of the main carrier amplifier. We have analyzed the operation and efficiency of the DDPA. The measured results show clearly that the DDPA delivers a flat efficiency range and good digital predistortion (DPD) linearization performance.

II. Analysis of Double Doherty Power Amplifier

Fig. 1 shows the schematic diagram of the proposed DDPA, which consists of two-stage carrier and peaking amplifiers. The driving and main carrier amplifiers are constructed with class-AB amplifiers. For the peaking amplifier, a class-C amplifier and a DPA are employed as the driving and main peaking amplifiers, respectively. The DPA consists of a class-B carrier cell and a class-C peaking cell to minimize the power consumption before the saturation of the main carrier amplifier. Also, the driving peaking amplifier biased to class-C plays an important role as a switch to make the carrier cell of the main peaking amplifier turn on or off.

The operation of the DDPA can be analyzed by regarding main carrier and peaking amplifiers as ideal current sources and the driving peaking amplifier as a switch. Fig. 2 shows the equivalent circuits at various operation regions. Although the DDPA has a two-way Doherty structure, the operation of the DDPA can be separated into three regions, which consist of low-, medium-, and high-power regions.

At low-power regions ($0 < V_{in} < V_k$), only the main carrier amplifier is turn-on since the driving peaking amplifier biased to class-C is in the OFF state and, therefore, the carrier cell of the DPA is turned off and the main peaking amplifier is regarded as an open circuit, as shown in Fig. 2(a). When the

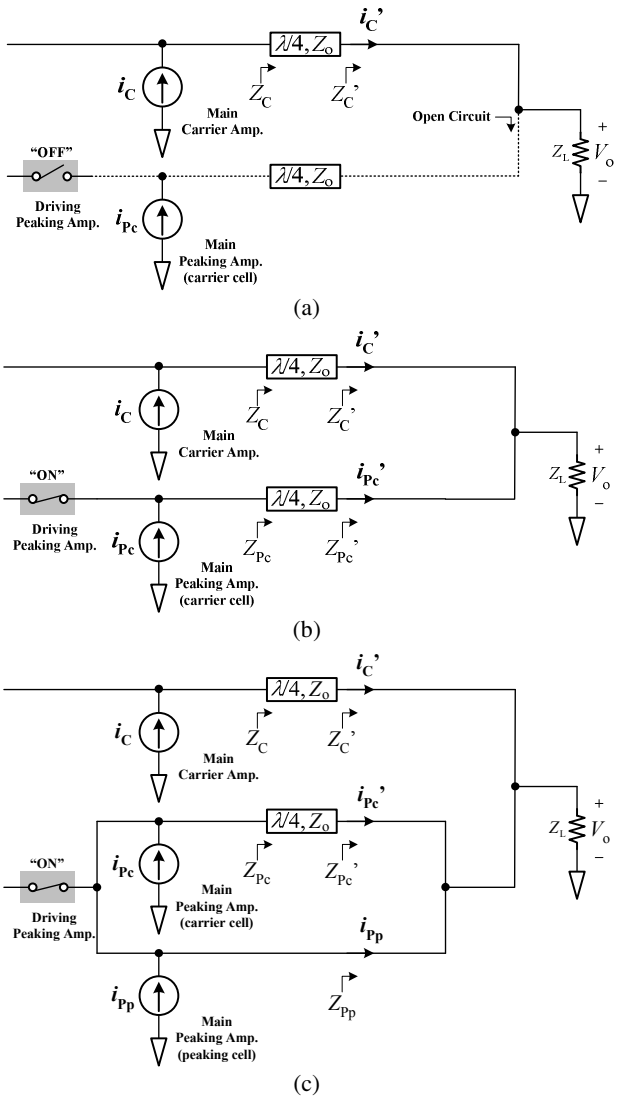

Fig. 2. Equivalent circuits of the DDPA at each operation region; (a) low- (b) medium-, and (c) high-power regions.

main carrier amplifier is saturated, the switch of the driving peaking amplifier transits to the ON state. At medium-power region ($V_k < V_{in} < V_{max}/2$), therefore, the main carrier amplifier is saturated and the carrier cell of the main peaking amplifier is turned on, as shown in Fig. 2(b). At high-power region ($V_{max}/2 < V_{in} < V_{max}$), the main carrier amplifier and the carrier cell of the main peaking amplifier are both in the saturation. The peaking cell of the main peaking amplifier is turned on and then all amplifiers are saturated, as shown in Fig. 2(c). Finally, the double Doherty operation is achieved by the additional Doherty operation of the main peaking amplifier after the saturation of the main carrier amplifier. Also, a flat efficiency range can be obtained by the double Doherty operation. Fig. 3(a) and (b) show the fundamental voltage and current characteristics and the load impedances of the DDPA according to input drive voltage, respectively. The efficiency of the DDPA at each region in Fig. 3(c) can be given by

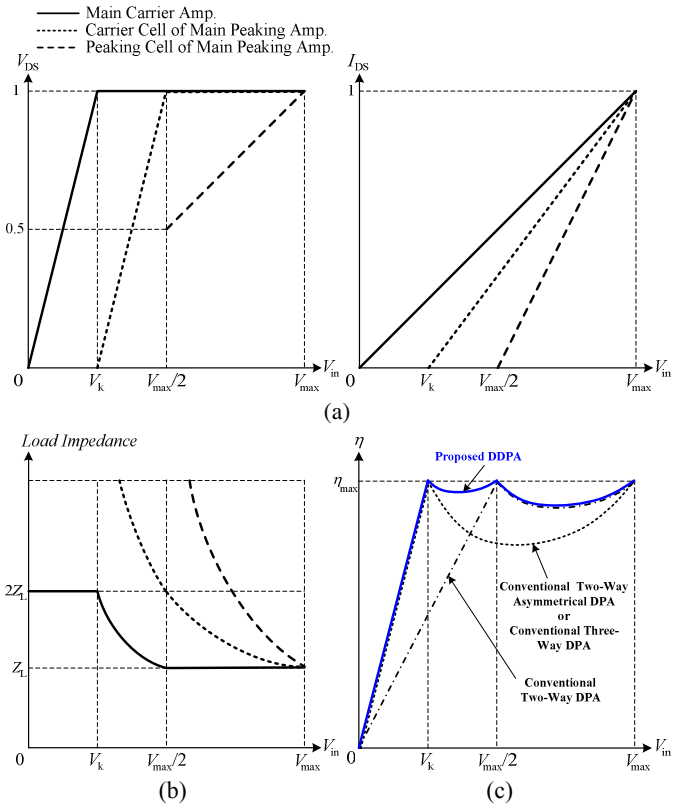

Fig. 3. (a) Fundamental voltage and current, (b) load impedance, and (c) efficiency of the DDPA according to input driving voltage.

$$\eta = \begin{cases} \eta_{\max} \times \dfrac{2(v_{in}/V_{\max})^2}{3(v_{in}/V_{\max})-1}, & \dfrac{V_{\max}}{2} \le v_{in} \le V_{\max} \\ \eta_{\max} \times \dfrac{2(v_{in}/2V_k)^2}{3(v_{in}/2V_k)-1}, & V_k \le v_{in} \le \dfrac{V_{\max}}{2} \\ \eta_{\max} \times \dfrac{v_{in}}{2V_k}, & 0 \le v_{in} \le V_k \end{cases} \quad (1)$$

where

$$V_k = \frac{5V_{\max}}{10+\beta(3+\beta)} \text{ and } \beta = \frac{\alpha \cdot 10^{\frac{\alpha}{20}}}{3}.$$

The v_{in} and V_{max} are the input voltage and the maximum input voltage, respectively, and is the saturation power difference between the main carrier and peaking amplifiers.

III. Implementation and Experimental Results

Fig. 4 shows the full schematic of the proposed DDPA. Compared to multi-stage DPA with specific impedances of λ/4 impedance transformers as the power combiner [3], [7], the power combiner of the DDPA is simply implemented with offset line ($_{p2}$) and λ/4 impedance transformers (50 Ω and 35 Ω). The driving carrier and peaking amplifiers have been implemented using RFHIC RT233 2-W GaN HEMTs. The gate bias voltages of the driving carrier and peaking amplifiers

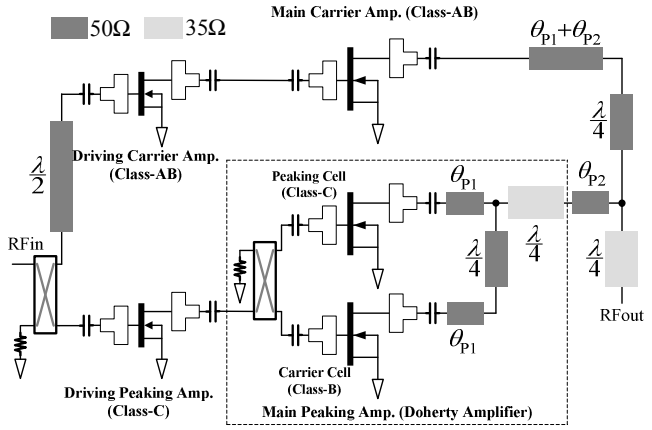

Fig. 4. Full schematic of the proposed DDPA.

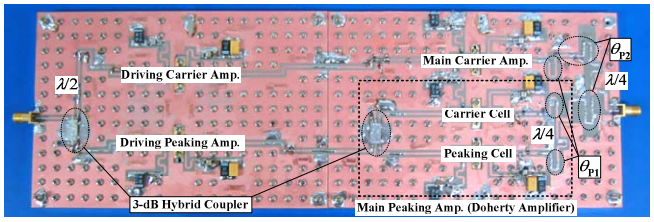

Fig. 5. Photograph of the fabricated DDPA.

(V_{GSDC} and V_{GSDP}) have been set to a class-AB bias of -1.60V (quiescent current, I_{DQ}=50 mA) and a class-C bias of -3.46 V, respectively, with a drain bias voltage (V_{DD}) of 28 V. The main carrier and peaking amplifiers have been fabricated with Cree CGH40010 10-W GaN HEMTs. The V_{GS} of the main carrier amplifier has been set to a class-AB of -2.31 V (I_{DQ}=50 mA) with a V_{DD} of 28 V. The V_{GS} of the carrier and peaking cells of the DPA used as the main peaking amplifier (V_{GSPC} and V_{GSPP}) have been set to a class-AB bias of -3.36 V (I_{DQ}=10 mA) and a class-C bias of -4.01 V, respectively, with a V_{DD} of 28 V to reduce power consumption when the carrier cell of the main peaking amplifier is turn-off. To reduce the memory effects, the drain bias circuits incorporated a λ/4 bias line and several decoupling capacitors. The optimum lengths of the $_{P1}$ and $_{P2}$ were the 0.28λ and 0.36λ of the 50 Ω transmission lines, respectively. Fig. 5 shows the photograph of the fabricated DDPA. The implemented DDPA has been tested using a continuous wave (CW) and a one-carrier WCDMA signal with a PAPR of over 9 dB at 2.14 GHz. The efficiency and linearity of the DDPA have been optimized at approximately 9-dB BOP region to satisfy the needs of the WCDMA systems.

Fig. 6 shows the measured drain currents of the DDPA for a CW at 2.14 GHz. Since the driving peaking amplifier is used as a switch to control the main peaking amplifier, the driving peaking amplifier is turn-on at a 9-dB BOP. From the results, the carrier and peaking cells of the main peaking amplifier are turn-on at near 9-dB and 6-dB BOP. The measured drain efficiency and gain characteristics of the DDPA for a CW are shown in Fig. 7. The DDPA delivers three efficiency-peaking

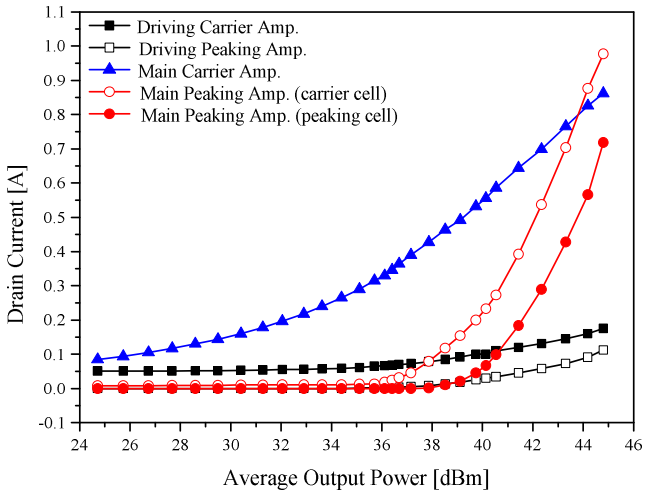

Fig. 6. Measured drain currents of the DDPA for a 2.14-GHz CW.

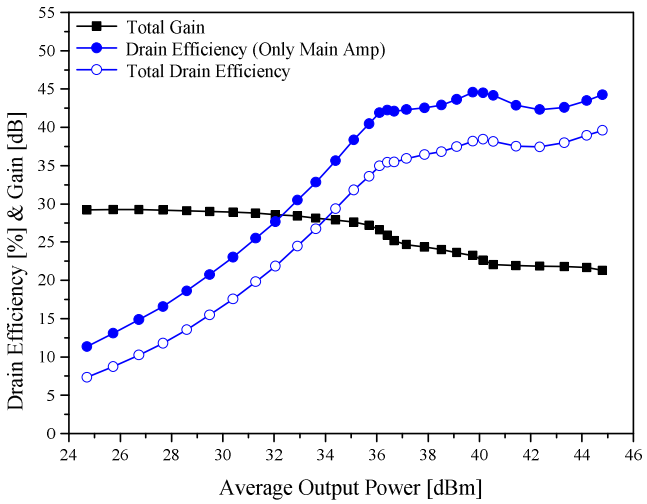

Fig. 7. Measured drain efficiency and gain characteristics of the DDPA for a 2.14-GHz CW.

TABLE I
MEASURED RESULT SUMMARY OF THE PROPOSED ADPA ACCORDING TO EFFICIENCY-PEAKING POINTS FOR A CW.

Contents		First	Second	Third
P_{out} [dBm]		36.1	39.8	44.8
Drain Efficiency [%]	Main Amp.	41.9	44.6	44.2
	Total	35.0	38.2	39.6
Gain [dB]		26.6	23.2	21.3

points by the double Doherty operation, and the the measured results are summarized in Table I. The first efficiency-peaking point is obtained at an average output power (P_{out}) of 36.1 dBm with a total drain efficiency of 35.0 % and a total gain of 26.6 dB. The second and third points are achieved at a P_{out} of 39.8 dBm and 44.8 dBm, respectively.

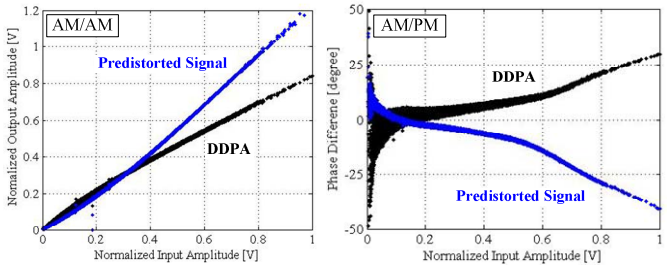

Fig. 8. Measured AM/AM and AM/PM characteristics of the DDPA and predistorted signal for a one-carrier WCDMA signal.

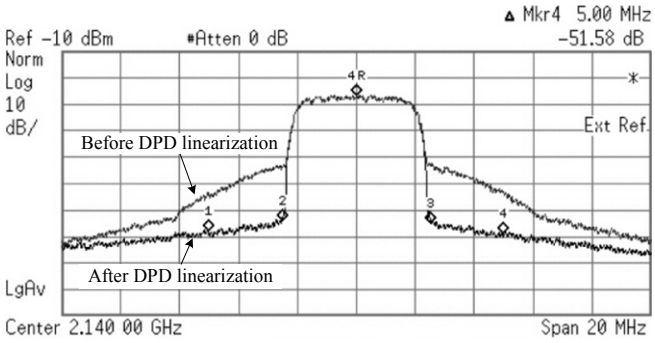

Fig. 9. Measured PSDs of the DDPA before and after DPD.

We have employed the memory DPD technique to satisfy the linearity specification. The 11th-memoryless polynomial characterizes the behavioral model of the DDPA and the entries in the AM/AM and AM/PM lookup tables (LUTs) and the coefficients of the memory system are determined by the recursive least square (RLS) algorithm via MATLAB [9]. Fig. 8 shows the measured AM/AM and AM/PM of the DDPA and predistorted signal for a one-carrier WCDMA signal. Fig. 9 depicts the measured power spectral densities (PSDs) before and after DPD linearization at a P_{out} of 34.5 dBm. The ACLR at ±5 MHz offset after linearization is below -51 dBc, which satisfy the linearity specification (an ACLR of below -45 dBc). The measured results are summarized in Table II. After DPD linearization, the DDPA delivers a total drain efficiency of 27.6 % and a total gain of 27.6 dB.

IV. Conclusions

We propose a new DDPA with a flat efficiency range, which consists of two-stage carrier and peaking amplifiers. By employing the two-way DPA as the peaking amplifier, three efficiency-peaking points are achieved since the additional Doherty operation of the main peaking amplifier is obtained after the saturation of the main carrier amplifier. The driving peaking amplifier with class-C bias keeps the carrier cell of the DPA turning off before the saturation of the main carrier amplifier. To verify our methods, the driving and main amplifiers were designed with 2-W and 10-W GaN HEMTs, respectively, at 2.14 GHz. For a CW, three efficiency-peaking points were at about 9-, 5-, and 0-dB BOPs with a drain efficiency of over 42 %. For one-carrier WCDMA signal, the DDPA delivers good DPD linearization performance. Thus, the proposed DDPA can be a promising solution to deliver a flat efficiency characteristic over a wide output power range.

TABLE II
Measured Result Summary of the DDPA Before and After DPD Linearization.

Contents		Before	After
Gain [dB]		27.4	27.6
Drain Efficiency [%]	Main Amp.	34.2	33.6
	Total	28.3	27.6
ACLR [dBc]	-/+2.5MHz Offset	-26.9/-26.2	-46.9/-47.7
	-/+5MHz Offset	-36.2/-35.9	-50.9/-51.6

Acknowledgement

This work was supported in part by the National Center for Nanomaterials Technology (NCNT), by the BK21 program, and by WCU (World Class University) program through the National Research Foundation of Korea funded by the Ministry of Education, Science and Technology (Project No. R31-2008-000-10100-0).

References

[1] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic´, N. Pothecary, J. F. Sevic, and N. O. Sokal, "Power amplifiers and transmitters for RF and microwave," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 3, pp. 814-826, Mar. 2002.

[2] Y. Yang, J. Cha, B. Shin, and B. Kim, "A fully matched N-way Doherty amplifier with optimized linearity," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 3, pp. 986-993, Mar. 2003.

[3] N. Srirattana, A. Raghavan, D. Heo, P. E. Allen, and J. Lasker, "Analysis and design of a high-efficiency multistage Doherty power amplifier for wireless communications," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 3, pp. 852-860, Mar. 2005.

[4] I. Kim, J. Cha, S. Hong, J. Kim, Y. Y. Woo, C. S. Park, and B. Kim, "Highly linear three-way Doherty amplifier with uneven power drive for repeater system," *IEEE Microw. Wireless Compo. Lett.*, vol. 16, no. 4, pp. 176-178, Apr. 2006.

[5] J. Y. Lee, J. Y. Kim, J. H. Kim, K. J. Cho, and S. P. Stapleton, "A high power asymmetric Doherty amplifier with improved linear dynamic range," in *IEEE MTT-S Int. Micro. Symp. Dig.*, 2006, pp. 1348-1351.

[6] Y. S. Lee, M. W. Lee, and Y. H. Jeong, "Linearity improvement of three-way Doherty amplifier using power tracking bias supply method," *Microw. Opt. Tech. Lett.*, vol. 50, no. 3, pp. 728-731, Mar. 2008.

[7] M. J. Pelk, W. C. E. Neo, J. R. Gajadharsing, R. S. Pengelly, and L. C. N de Vreede, "A high-efficiency 100-W three-way Doherty amplifier for base-station applications," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 7, pp. 1582-1591, Jul. 2008.

[8] Y. S. Lee, M. W. Lee, and Y. H. Jeong, "Unequal-cells-based GaN HEMT Doherty amplifier with an extended efficiency range," *IEEE Microw. Wireless Compo. Lett.*, vol. 18, no. 8, pp. 536-538, Aug. 2008.

[9] M. W. Lee, Y. S. Lee, S. H. Kam, and Y. H. Jeong, "A wideband Digital predistortion for highly linear and efficient GaN HEMT Doherty power amplifier," *Microw. Opt. Tech. Lett.*, vol. 52, no. 2, pp. 484-487, Feb. 2009.