Design of a Class F Power Amplifier

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Abstract— A Class F power amplifier (PA) at 2.5 GHz has been designed and fabricated. Test results show 15.7 dB gain with 75.75% power added efficiency (PAE), at an input level of 25 dBm. The design procedure is presented, with various issues illustrated and addressed. A new method is proposed to obtain the optimum load and source impedances without iterations, which would usually be necessary.

1. INTRODUCTION

The Class F amplifier is a reduced angle amplifier with load harmonic modulation control to shape the drain voltage in a way that it does not or rarely does coincide with drain current, thus greatly reducing the power dissipated by the device, and hence further increasing the efficiency without having to drive the amplifier into compression. The theory has been well explained by Cripps [1] and Raab [2].

Design of a Class F amplifier involves matching network design at the fundamental frequency, and load harmonic tuning network design up to certain order harmonics. The common practice is to present a short circuit at the even order harmonics, and an open circuit at the odd order harmonic. Note that shorting the even order harmonics has its sound theoretical foundation, while the principle regarding odd order harmonics is just a folklore notion, the insight on which has been discussed by Cripps [1]. In most cases only the second and third order harmonics are considered, since higher order harmonic control would lead to more complexity and possibly further loss [3]. Some published papers have reported Class F power amplifiers with efficiency around 80% at 2 GHz or lower frequencies [4, 5]. This paper presents the design of a Class F power amplifier at 2.5 GHz, which is required to deliver at least 5 W output power P_{out} with no more than 25 dBm input power.

2. DESIGN

The transistor chosen is Cree CGH40010 GaN HEMT. It is biased at $V_{DD} = 28$ V, $I_{DQ} = 200$ mA. A corresponding large signal model is provided by Cree, Inc. The software used is AWR Microwave Office. Taconic *ORCER RF-35* is chosen to be the board material with a thickness of 60 mils, while the metal is 1 oz copper. RF-35 has a stable ϵ_r of 3.5 over a wide frequency band from 2 GHz to 10 GHz, and a dissipation factor of 0.0018 at 2.5 GHz. The design procedure is illustrated in the following subsections.

2.1. Prototyping Using Ideal Components

Usually the first step would be to get the optimum load impedance that induces maximum saturation power, and the source impedance that presents maximum transistor gate voltage. In the case of this design however, these parameters are already provided in the data sheet — at the fundamental frequency $f_0 = 2.5$ GHz, optimum load impedance Z_L is $6.37-j0.1$, and optimum source impedance Z_S is $4.0-j4.0$.

If it were a Class A amplifier, one would be able to start designing the matching network right away given Z_L and Z_S. However, since the Class F amplifier design involves load harmonic control, which undoubtedly would change the load impedance at the fundamental frequency f_0, it is reasonable to design the harmonic control circuitry, and then complete additional load circuitry that presents Z_L at f_0 to the transistor output.

It is beneficial to first build up a prototype with lossless transmission lines (TLs), and ideal lumped components, just to verify that Z_L and Z_S indeed produce the required performance. Figure 1 shows the load network, where TL3 and TL4 together presents an open circuit to the drain at the $3f_0$, TL5 works as the RF choke and also presents a short circuit to the drain at $2f_0$. The rest of the circuit makes sure that Z_L is presented to the transistor drain at f_0.

The source matching is a basic process thus is not shown here. The P_{out}/PAE vs. input power (P_{in}) plot is shown in Figure 2. It is observed that maximum efficiency of this configuration is 84.34%, with P_{out} more than 39 dBm. However it should be noted that at that point the amplifier has already reached well into saturation.

2.2. Design with Lossy Components

As the design evolves to lossy components, several problems need to be addressed. One is that lumped components of certain values at such high frequencies might not be available. For example, in the matching network prototype the DC blocking capacitors have a value of 1000 pF. This is already close to the upper bound of chip capacitors at 2.5 GHz. Thus they should be replaced with smaller, more practical ones. However the reason why such large capacitance was chosen in the first place is to make sure its impedance is small enough at f_0 to be ignored. Once the capacitance is changed to a much smaller value, the matching network needs to be redesigned. Therefore it is suggested this should be considered at the stage of ideal circuit prototyping to save some repetitive work. In this design, 0.7 pF is chosen as the DC blocking capacitance, and it is considered when designing the matching networks.

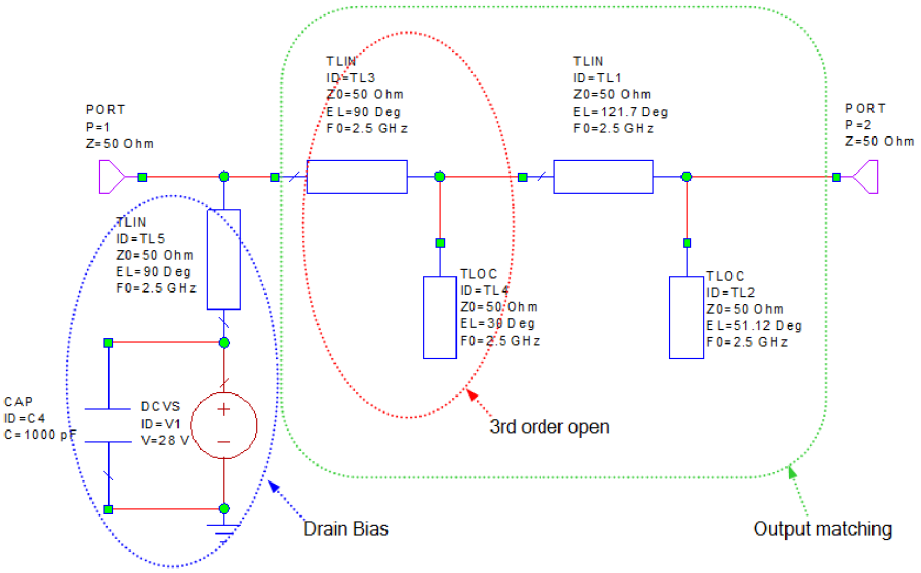

Figure 1: Ideal load network.

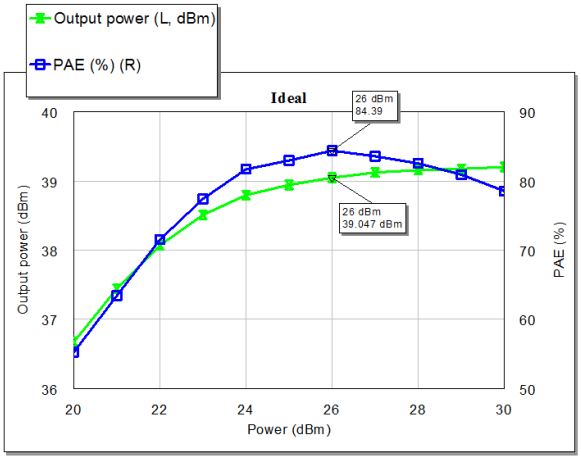

Figure 2: P_{out} and PAE vs. P_{in} of the amplifier prototype using ideal components.

Another problem is the effect of the microstrip line junction on the lengths of the lines connected to it. Figure 3 shows four microstrip lines connected by a junction component named "MCROSS" in Microwave Office. When designing the impedance network four such TLs are connected to an artificial "point", which has no physical dimensions whatsoever. But in practice it is necessary to investigate the junction.

Figure 4 is to explain how to connect several lines together. W1 to W4 are widths of the connected lines, whose reference planes are the black dashed lines, meaning the "MCROSS" component is bounded by the black dashed lines. However, in practice the artificial "point" mentioned above is usually transformed into two reference planes represented by the red dashed line. For this reason, if the line connected to port 1 of the junction has a length of L in the design, once it is connected in Microwave Office with "MCROSS", 0.5·W4 has to be subtracted from L. The same principle applied for all other ports.

With the problems above solved, the design becomes a simple task. However, tuning or optimization is inevitable after the initial design, for small variations of TL length can affect the performance severely at GHz frequencies. Using the optimizer in Microwave Office, it is fairly easy to make the matching network present the desired impedance at a certain frequency.

For the load network, first the harmonic control circuit is tuned, followed by optimization at f_0. Note that short at 2nd order harmonic can be quite accurate, while open circuit at 3rd order harmonic may not necessarily yield infinite impedance. The best value in this example is 2200 Ω, which is good enough to get a high efficiency. The simulation result is shown in Figure 5, where

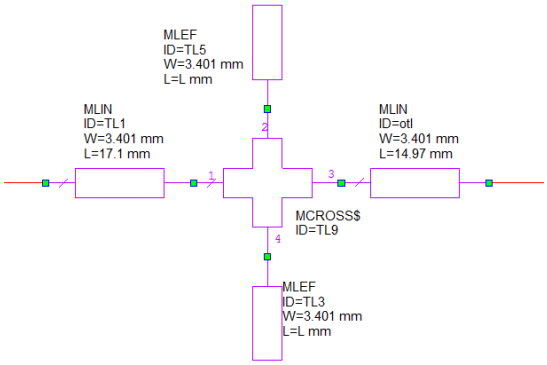

Figure 3: Four microstrip lines with a junction.

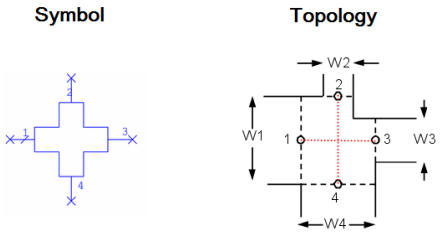

Figure 4: Illustration of the microstrip line junction.

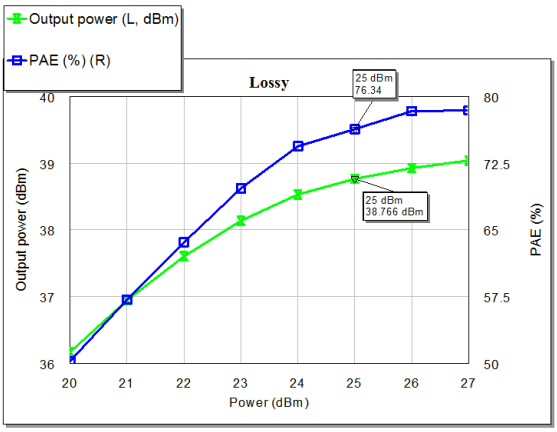

Figure 5: P_{out} and PAE vs. P_{in} of the amplifier using lossy components.

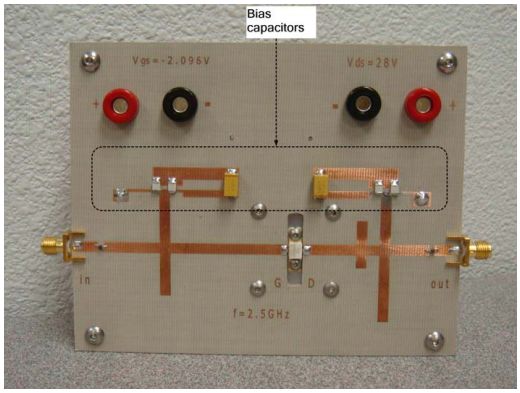

Figure 6: Final board.

it is observed that both power and efficiency are lower than their counterparts in the ideal case. Microwave Office is used for the PCB design. And the final board is shown in Figure 6. Note that different capacitors are connected in parallel in the bias circuits so that their resonances can be cancelled out, and sudden changes of the bias voltages can be prevented.

3. MEASUREMENTS

Measurements are performed at f_0, and the results are shown in Table 1. With these measurement results, the DC power dissipated by the transistor is 15.4 W, and the PAE is 75.75%.

Table 1: Measurement results.

P_{in} (dBm)	Gain (dB)	P_{out} (dBm)	$I_{drain_{dc}}$ (A)	$V_{drain_{dc}}$ (V)
25	15.785	40.785	0.55	28

4. NEW METHOD TO OBTAIN OPTIMUM IMPEDANCES

Although in this design the optimum impedances are readily available from the datasheet, one can always obtain them by performing load pulling and source pulling. This is usually a back-and-forth process, since one might not be able to pull both sides simultaneously.

To avoid this process, one could reason that it is the duty of the load network to sustain maximum drain voltage swing just when the drain current swing reaches its maximum value, and the load impedance that makes this happen is the optimum load impedance. With this principle, pulling can be performed without repetition whether in a simulator or with actual pulling devices. In the simulator, first, a voltage source is connected directly to the transistor gate to make sure the drain current reaches its maximum swing. And then, load pull can be performed to get the Z_L. Finally, the load impedance is set to Z_L and source pull is performed to get Z_S.

Regarding the final step, if one wishes to measure the input large signal impedance of the transistor and use the conjugate of that value as Z_S, it also works. There is however an interesting point here. At the input side of the amplifier, what matters is how much gate voltage swing is available given a certain input power. While what conjugate matching guarantees is maximum power transfer. These are actually two different problems. Suppose the large signal admittance of the transistor is $Y_{in} = G_{in} + jB_{in}$, it is not difficult to deduce the relation between gate power P_g and gate voltage V_g, as shown in Equation (1), from which one can tell that maximum gate power indeed corresponds to maximum gate voltage swing.

$$P_g = 0.5 \cdot |V_g|^2 \cdot G_{in} \tag{1}$$

5. CONCLUSION

The design procedure of a Class F amplifier has been presented, with various practical design issues addressed. A novel means of obtaining optimum impedances is discussed, with the relation between transistor gate voltage and power elucidated.

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