

FPGA-Based Set-Up for RF Power Amplifier Dynamic Supply with Real-Time Digital Adaptive Predistortion

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Abstract — This paper presents an exhaustive description of a field programmable gate-array (FPGA) based set-up for envelope tracking and dynamic biasing of RF power amplifiers (PA). The system includes digital adaptive predistortion (DAPD) and gain compensation deployed in a FPGA device. For testing purposes a GaN HEMT RF PA operating at 3.5 GHz was considered. Preliminary experimental results are provided showing the DAPD compensate for the steady-state PA nonlinear distortion arising as a consequence of varying the power supply.

Index Terms — Dynamic power supply, envelope tracking, digital adaptive predistortion, FPGA, power amplifiers.

I. INTRODUCTION

Reducing energy consumption to cope with the steadily rising energy cost and global CO₂ emission has become one of the main objectives worldwide. Since the power amplifier (PA) is one of the most power hungry devices in communications, several efforts are being made to design energy-efficient or ‘green’ linear amplifiers. Therefore, operating with linear Class-A PAs at significant power back-off levels, to linearly amplify nonconstant envelope modulated signals, is no longer a desirable solution since it results power inefficient.

Thanks to the intensive processing capabilities offered by the ‘always faster’ digital signal processors, some power supply control architectures with great potential for high-efficiency operation have been revived. The PA drain supply modulation is carried out using techniques such as envelope elimination and restoration (EE&R) [1] and envelope tracking (ET) [2],[3] in conjunction with digital predistortion (DPD). In addition, in certain transmission systems where the required transmission power is variable (satellite and aeronautical communications in function of the distance, or base stations in function of the number of users), ‘smart supply’ techniques have been applied [4],[5].

In a first approach, this paper presents an insight view of a FPGA-based set-up required for introducing drain supply modulation. This set-up is then used for testing the capability of the implemented real-time LMS-based DAPD for compensating the gain and nonlinear distortion

that appears when changing the power supply of a GaN PA. One of the main advantages of the DAPD is that is capable to compensate for the PA nonlinear distortion in a hot manner, that is, no previous training is required. Moreover, it is scalable and additional modules to compensate for PA memory effects can be easily included.

II. DESIGN OF THE EXPERIMENTAL SET-UP

Fig. 1 shows the block diagram of the implemented hardware set-up. Baseband processing was carried out in a Xilinx Virtex-4 FPGA together with two 14 bits DACs and ADCs.

A. Digital ‘Baseband to IF’ Set-up

The In-phase and Quadrature components of the modulated signal to be transmitted $x(n) = x^I(n) + jx^Q(n)$ are defined in (1)

$$\begin{aligned} x^I(n) &= a(n) * h^{RRC}(n) = \sum_{k=-\infty}^{\infty} a(k) \cdot h^{RRC}(n-k) \\ x^Q(n) &= b(n) * h^{RRC}(n) = \sum_{k=-\infty}^{\infty} b(k) \cdot h^{RRC}(n-k) \end{aligned} \quad (1)$$

where $h^{RRC}(n)$ is the impulse response of the root-raised cosine (RRC) filter and $a(n)$, $b(n)$ are the symbols of the M-QAM modulation scheme ($u(n) = a(n) + jb(n)$). For example, considering $M=16$, $a(n), b(n) \in \{-3, -1, 1, 3\}$. Then, the input complex baseband signal is predistorted as it is described in (2)

$$\begin{aligned} x_{PD}(n) &= x(n) \cdot G_{LUT}^*(|x(n)|) \\ x_{PD}(n), x(n), G_{LUT}(\cdot) &\in \mathbb{C} \end{aligned} \quad (2)$$

being G_{LUT} a complex gains stored in the look-up table (LUT) that depends on the modulus of the complex input data. The predistortion gains stored in the Pre-Distortion LUT (see Fig. 1) are adaptively updated in the FPGA by means of an LMS algorithm as it is described in (3)

$$G_{LUT}^{(new)}(|x(n)|) = G_{LUT}^{(old)}(|x(n)|) + \mu \cdot x(n) \cdot e^*(n) \quad (3)$$

The error $e(n)$ in the Post-Distortion LUT is computed as $e(n) = x(n) - \hat{x}(n)$, where $\hat{x}(n)$ is the estimated input

after post-distortion (see Fig. 1). Further details on the DAPD functioning can be found in [6].

The modulus of the predistorted M-QAM signal ($|x_{PD}(n)|$) is sent to the DAC 1, while the predistorted M-QAM signal is modulated at the IF frequency ($x_{IF}(n)$) and then sent to the DAC 2,

$$x_{IF}(n) = x_{PD}^I(n) \cos(\Omega_x n) + x_{PD}^Q(n) \sin(\Omega_x n) \quad (4)$$

with $\Omega_x = 2\pi f_x / f_s$ and where f_x is the frequency in the analog domain and f_s the sampling frequency of the DACs and ADCs.

B. Analog 'IF to RF' Set-Up

In order to operate at the frequency of 3.5 GHz two upconversion stages have been used, as depicted in Fig. 1. In a first approach, the interpolation filter in DAC 2 was set to a high pass characteristic in order to capture the IF signal. Then, the analog output signal at IF was band pass filtered in order to reject its alias. Fig. 2 shows the power spectra of the transmitted signal at different stages of the transmitter. To remove the unwanted image of the IF signal we cascaded a power splitter and an IQ modulator.

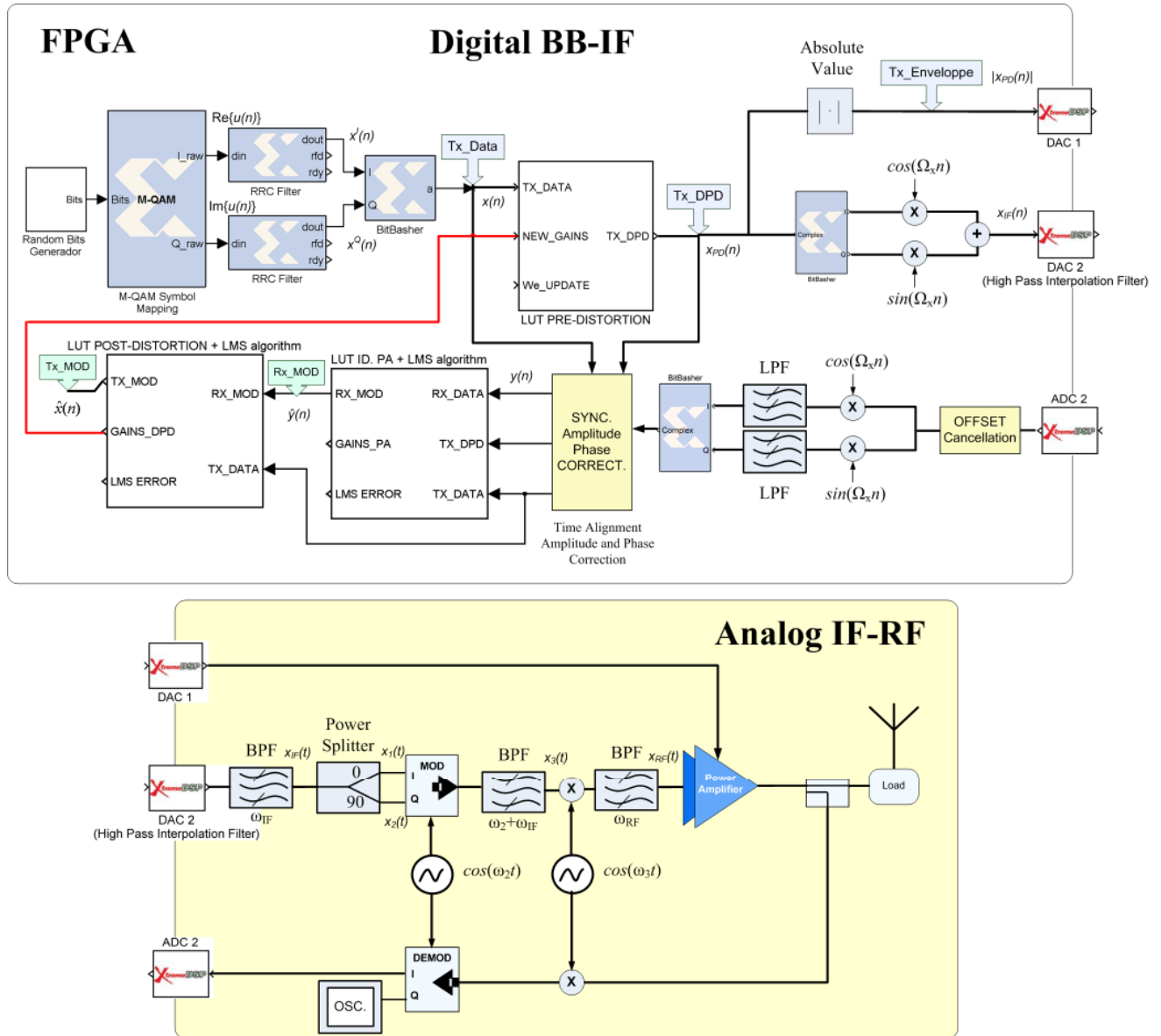


Fig. 1. Block diagram of the FPGA based set-up for envelope tracking and dynamic supply purposes.

As it is observed in Fig. 2, after the IQ modulator we obtained a modulated signal at the $f_2 + f_{IF}$ frequency where the IF image was removed. Finally, after the second mixing stage and band pass filtering at the RF frequency, we obtained the desired RF signal at $f_{RF} = f_2 + f_{IF} + f_3$. Table I lists the frequency values considered for operating at the RF frequency of 3.5 GHz.

C. Envelope calculation

The envelope of the baseband signal is calculated in the FPGA and then sent to DAC 1, as it is shown in Fig. 1. To calculate the modulus of the baseband signal we mapped the squared root function in a LUT of 2^{11} bins. In addition, a memory buffer was used to synchronize the envelope with the modulated IF signal (in DAC 2), as it can be shown in Fig. 3 considering a 16-QAM test signal.

III. DYNAMIC SUPPLY AND NONLINEAR DISTORTION COMPENSATION: EXPERIMENTAL RESULTS

A. PA performance under variable power supply

For testing purposes we used a Cree Inc. Eval. Board CGH40010-TB (GaN HEMT transistor, 10 W CW) at 3.5 GHz and a 4 MHz bandwidth 16-QAM modulated test signal. Experimental tests showed that the relation between the V_{DS} and the PA gain variation is approximately 2:1. Therefore, if V_{DS} is reduced 6 dB (i.e. a step from 28 V to 14 V) then, a drop of gain of 3 dB is measured. When V_{DS} is reduced the PA operates in a more nonlinear region and then this has to be compensated by means of the DADP.

B. Results of DAPD real-time compensation

To test the DAPD compensation capabilities different power supply conditions for the PA were considered. Therefore, we evaluated the DAPD performance for the V_{DS} extreme values of 28 V and 3.5 V and with $V_{GS} = -2.8$ V (class A mode). The objective was to operate always in the same nonlinear region (determined by the ACPR levels and the AM-AM characteristic) independently of the specific drain voltage applied. Then, the DAPD had to be capable to adaptively converge and compensate for the PA nonlinear behavior. Fig. 4 and Fig. 5 show the DAPD capability to linearize the PA despite the power supply changes. In addition, each of the drain voltages determines the actual output power for having linear amplification (after DAPD compensation). Therefore, according to our experimental results, for transmitting at a mean output power of 26 dBm, the best power supply to use is $V_{DS} = 28$ V. While for transmitting at 17 dBm mean output power, a drain voltage of $V_{DS} = 3.5$ V is enough and it results much more efficient. Finally, Fig. 6 shows the DAPD linearity performance with the PA operating in a different operating mode (class AB, $V_{GS} = -3.4$ V).

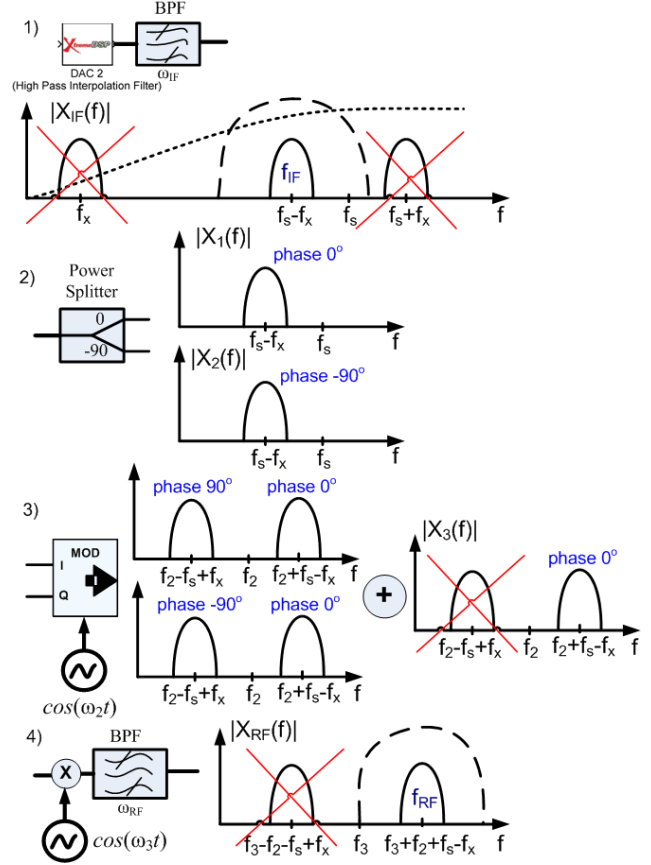


Fig. 2. Power spectra of the transmitted signal at different stages.

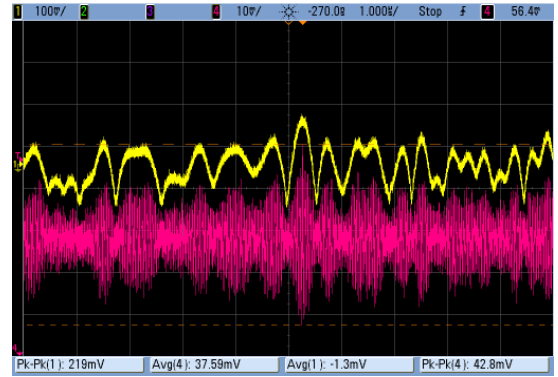


Fig. 3. Oscilloscope capture of the modulated signal at IF (red) and its corresponding baseband envelope (yellow).

TABLE I
FREQUENCY VALUES IN OUR HARDWARE SET-UP

FREQUENCY	VALUE	FREQUENCY	VALUE
Ω_x	$\pi/2$		
f_s	40 MHz	$f_{IF} = f_s - f_x$	30 MHz
f_x	10 MHz		
f_2	1950 MHz	$f_{RF} = f_3 + f_2 + f_{IF}$	3.5 GHz
f_3	1520 MHz		

V. CONCLUSION

The developed hardware set-up is intended for future implementation of an ET system where dynamic supply voltage will be considered. At this stage, we have evaluated and proved the capability of the real-time DAPD to compensate for nonlinear distortion in a scenario where the supply conditions of the PA are variable, and thus suitable for 'smart supply' applications.

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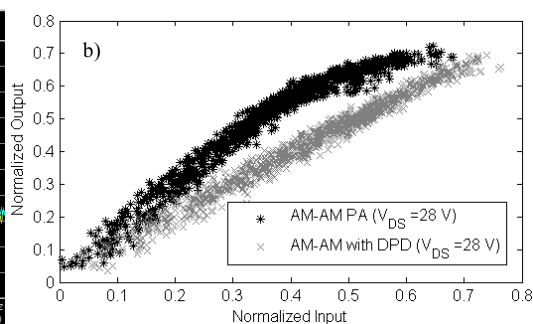
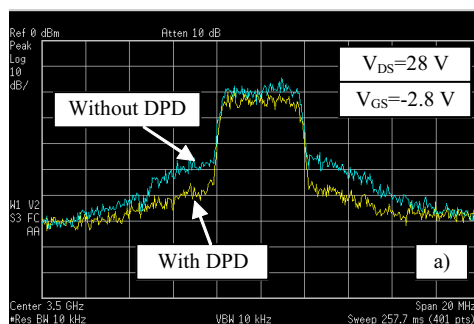


Fig. 4. Unlinearized and linearized class-A PA with 26 dBm mean output power: a) Output power spectra; b) AM-AM characteristic.

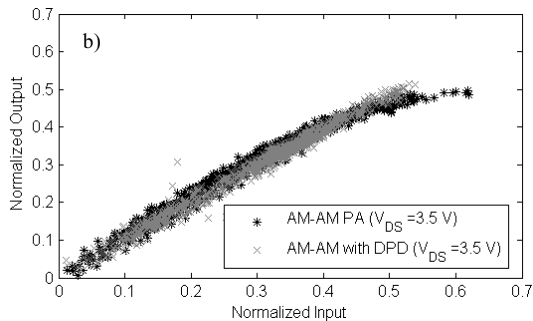
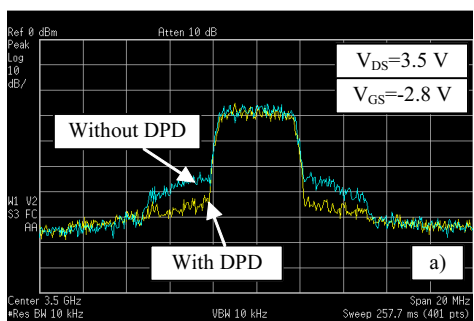


Fig. 5. Unlinearized and linearized class-A PA with 17 dBm mean output power a) Output power spectra; b) AM-AM characteristic.

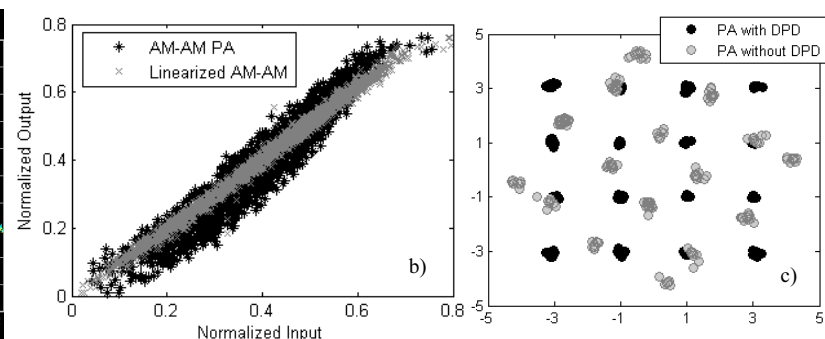
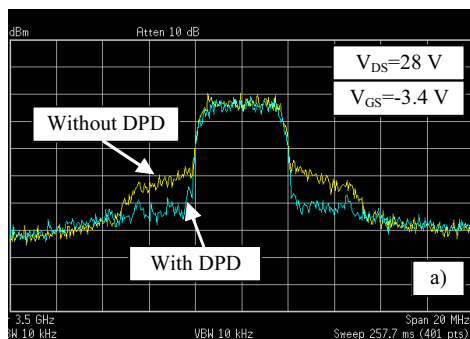


Fig. 6. Unlinearized and linearized class-AB PA: a) Output power spectra; b) AM-AM characteristic; c) 16-QAM constellation.