High Power, High Conversion Gain Frequency Doublers Using SiC MESFETs and AlGaN/GaN HEMTs

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***Abstract* — High power, high conversion gain microwave frequency doublers using wide bandgap semiconductor devices are developed. A method of determining the optimal harmonic terminations using accurate nonlinear computer models and load- and source-pull simulations is described. Synthesis of these impedances using matching and reflector networks have produced doublers with increased output power, conversion gain and very high suppression of the first and third harmonics. A SiC MESFET-based frequency doubler at f_o=2.00GHz producing up to 10.00dB conversion gain and 6.31 Watts $2f_o$ output power is presented. An AlGaN/GaN HEMT-based frequency doubler at f_o=3.33GHz producing up to 14.80dB conversion gain and 4.14W $2f_o$ output power is also presented. The second harmonic power measurements confirm the accurate predictions made by the nonlinear model.**

***Index Terms* — Frequency doubler, frequency multiplier, SiC MESFET, GaN HEMT, high power, harmonics, reflectors, load-pull, source-pull**

I. Introduction

Frequency multipliers play an important role in signal source generation and frequency conversion in microwave communication systems. Typically, a passive frequency multiplier is employed to multiply a signal source to the nth harmonic, followed by an output power amplifier (PA) for delivery to subsequent stages. While a nonlinear device such as a varactor diode may provide multiplication, this two-stage approach assigns constraints to the PA which include high gain and output power operation at the nth harmonic. One aspect of the development of active, high power frequency multipliers with high conversion gain is motivated by the desire to combine the functionality of the passive multiplier with the output PA. Such high conversion gain, high power active frequency multipliers permit elimination or relaxation of the PA requirements, thereby simplifying and improving the efficiency of the overall system.

Advances in wide bandgap semiconductor technologies such as silicon-carbide (SiC) and aluminum-gallium-nitride/gallium-nitride (AlGaN/GaN or GaN) have created new possibilities in high power, microwave integrated circuits. The manipulation of higher order harmonics in such devices has demonstrated improvements in power amplifier performance [1]. However, little work has been done in harmonic tuning for frequency multiplication in SiC MESFET and GaN HEMT devices [2]. This is due in part to the scarce availability of accurate nonlinear models which account for the dispersive effects inherent in these technologies, leaving measurement-based design strategies as the only option [3].

Several recent papers on frequency doublers have reported high conversion gain and moderate power levels [2],[4]-[7]. However none report power levels in excess of 1W at $2f_o$. In this work, high power, high conversion gain frequency doublers based on SiC MESFET and GaN HEMT technology are developed using precision nonlinear active device models. To the authors' knowledge, these are the first microwave frequency doublers utilizing these devices demonstrating the capability of producing >4W at $2f_o$. This appears, therefore, to be the highest microwave output power of any single transistor frequency multiplier to date.

An overview of frequency doubler performance parameters is given in Section II. The design strategy of the bias and load and source networks is described in Section III. Large-signal measured performance of the realized doublers are provided in Section IV. Lastly, Section V concludes this work.

II. Microwave Frequency Doubler and Device Overview

An unbalanced, single-transistor topology using harmonic reflection and matching networks is chosen for simplicity, low loss, cost and efficiency [8], [9]. Figure 1 illustrates a canonic realization of an ideal single-ended frequency doubler consisting of a high power active device coupled with performance-enhancing input and output networks.

The primary performance parameters under investigation for this frequency doubler are:

1. Output power at the second harmonic, Pout($2f_o$)
2. Conversion gain, CG($2f_o$)
3. Drain efficiency, ($2f_o$), and power added efficiency, PAE($2f_o$)
4. Suppression of unwanted f_o and $3f_o$ harmonics, Pout(f_o)/Pout($2f_o$) and Pout($3f_o$)/Pout($2f_o$).

In this work, the commercially available devices employed to realize the doublers are the CRF24010 10W SiC MESFET [10] and the CGH40010F 10W GaN HEMT [11] devices, both manufactured by Cree, Inc. The high power density and relative immaturity of these wide bandgap devices result in substantial self-heating and charge-trapping effects. These dispersive effects can lead to poor predictions of harmonic generation if not properly taken into consideration. Fortunately, a substantial effort has been made to develop

high-accuracy nonlinear models for both the SiC MESFET [12] and GaN HEMT devices [13] allowing for close performance predictions by the use of computerized design methods. The generalized circuit representation of the large-signal model for both devices is illustrated in Fig 1. The models and simulations presented here were performed employing the Agilent Advanced Design System (ADS) software package.

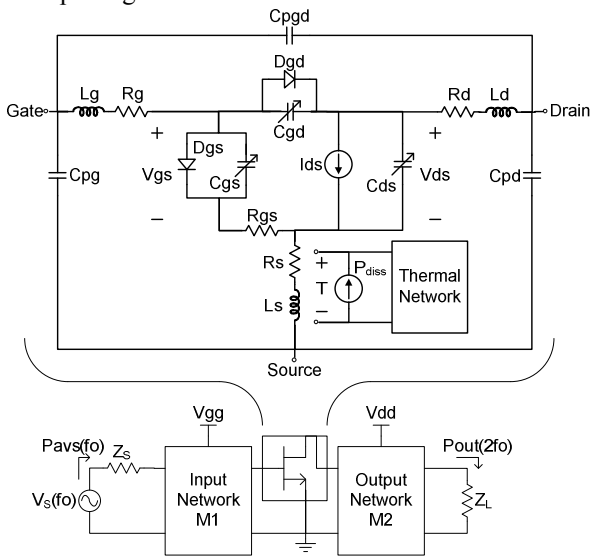

Fig. 1. Generalized single-ended high-power frequency doubler with large-signal model.

III. Design of High Power Frequency Doublers

The design of the SiC MESFET and GaN HEMT-based microwave frequency doublers is described in the ensuing paragraphs. Fundamental frequencies of 2.00GHz and 3.33GHz were employed for the SiC MESFET and GaN HEMT, respectively. The primary steps involved in the design are (a) selecting the appropriate device biasing, (b) determining the optimal source and load impedances which provide maximum Pout and CG, and (c) synthesizing these impedances into low-loss microstrip networks.

A. Device Biasing

Pinchoff bias is selected as the operating point of the SiC and GaN transistors for its numerous advantages. As shown in [14], pinchoff produces a half-wave rectified drain current waveform which is both rich in second and low in third harmonic content. Additionally, pinchoff produces no quiescent power dissipation, improving efficiency at low drive levels. Furthermore, the device has little gain at pinchoff resulting in stability under small-signal conditions. High drain-source voltage operation of the SiC and GaN devices allow for the increased generation of second harmonic power. A bias of Vgs=-11V, Vds=55V for the SiC MESFET and Vgs=-3.0V, Vds=28V for the GaN HEMT is selected.

In most practical cases, the predicted $2f_o$ harmonic will quickly deviate from ideal once parasitic and frequency dependent elements are considered [8], [9]. Therefore, biasing alone will not lead to significant output power nor conversion gain and harmonic terminations aiding the generation and delivery of $2f_o$ harmonic power are consequently essential.

B. Optimal Harmonic Load and Source Impedances

The optimal harmonic load and source impedances have been determined using harmonic load- and source-pull simulations in conjunction with highly accurate nonlinear device models [12], [13] implemented in ADS. A simplified schematic of the implementation for the case of two harmonics is shown in Fig. 2. This approach assumes no topology and is used as an analytical tool in investigating the effect of the harmonic impedances on device output. Due to the availability of the high-precision nonlinear models, harmonic load- and source-pull can be implemented in simulation and executed to provide extremely accurate, optimal results.

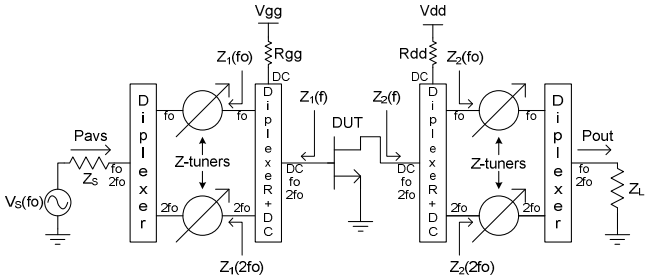

Fig. 2. Simplified schematic of harmonic load- and source-pull analysis simulation.

In Fig. 2, the ideal harmonic diplexer separates the signal path into two branches based on the specific frequencies at the input and output terminals of the device. Each branch is implemented with an impedance tuner to alter the port impedance at the particular harmonic of interest. In this procedure, the impedances $Z_1(f_o)$, $Z_1(2f_o)$ seen at the gate at fo and 2fo, respectively, and $Z_2(f_o)$, $Z_2(2f_o)$ seen at the drain are systematically swept about an *a priori* optimum in order to obtain the optimum output performance.

Although no assumption has been made about the network topology, harmonic reflector networks at both device ports can increase device performance through the constructive recycling of generated harmonics [8], [9]. A $2f_o$ reflector placed at an optimal phase offset from the device input can improve conversion gain through linear $2f_o$ amplification. Similarly, a f_o reflector at an optimal phase offset from the device output can heavily suppress unwanted f_o and $3f_o$ output and improve both $2f_o$ output power and gain through harmonic mixing at the drain.

The determined harmonic impedances for the SiC MESFET and GaN HEMT designs are shown in Fig. 3.

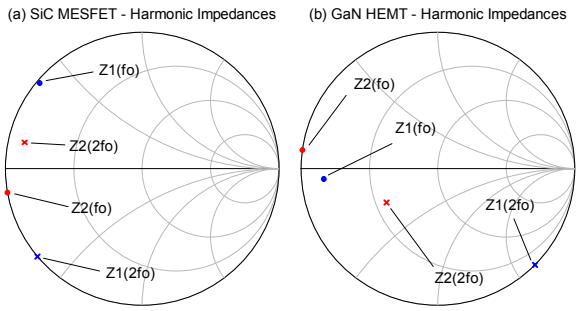

Fig. 3. Derived harmonic load and source impedances for the (a) SiC MESFET and (b) GaN HEMT.

C. Synthesis of the Load and Source Networks

External bias tees are used for the frequency doubler prototypes and consequently attention will be focused on realizing Z_1 and Z_2 at RF. Straightforward, low-loss, narrowband microstrip stub networks are used to realize Z_1 and Z_2. The synthesized circuit topology is shown in Fig. 4. Each input and output network as viewed from the device ports consists of two stages: a harmonic reflector and a stub matching network. The synthesized offset phase lengths with respect to f_o in degrees are tabulated in Table I for both the SiC MESFET and GaN HEMT designs.

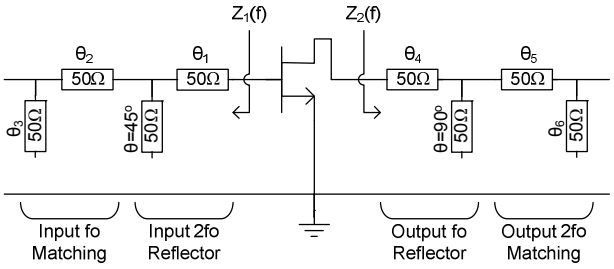

Fig. 4. Topology of the prototype SiC MESFET and GaN HEMT-based frequency doublers.

The networks were fabricated using Rogers RT/duroid 5880 microwave laminate. The reflector and matching network impedances are 50 which allow for safe reflection of the high power levels. The generation of excessive heat due to reflecting high power f_o signal back into the drain of the device prevented the use of higher impedance lines having higher Q. The use of a 120 f_o output reflector was attempted but resulted in a burned copper trace when subjected to high power operation. A photo of the GaN HEMT-based frequency doubler is shown in Fig. 5.

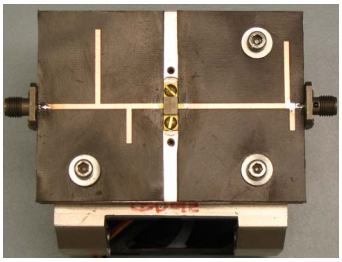

Fig. 5. Photo of GaN HEMT-based frequency doubler.

TABLE I
FREQUENCY DOUBLER TRANSMISSION LINE LENGTHS

Device	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6
SiC	80.00	73.47	83.60	175.00	15.25	37.50
GaN	56.16	50.21	109.74	179.33	7.45	24.03

IV. MEASUREMENTS AND CIRCUIT PERFORMANCE

The performance of the SiC MESFET- and GaN HEMT-based doublers were measured under a wide range of large-signal drive conditions and compared with simulated results.

The large-signal harmonic output power of the SiC MESFET and GaN HEMT-based doublers are shown in Fig. 6a and 6b, respectively. Additionally, the CG, and PAE for the $2f_o$ output are shown for both designs in Fig. 7a and 7b, respectively. A perusal of these results reveals that a maximum $Pout_{2fo}$ of 38.00dBm (6.31W) has been achieved for the SiC MESFET doubler. Similarly, a maximum $Pout_{2fo}$ of 36.17dBm (4.14W) has been achieved for the GaN HEMT doubler. Also, an examination of these curves determines that a good suppression of the f_o as well as the $3f_o$ output power is achieved. These measurements show good agreement with the simulations. Table II compares the doublers' maximum performance with that of recently published work.

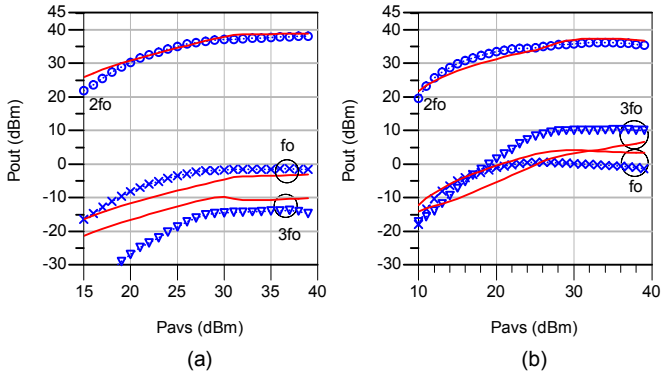

Fig. 6. Measured (symbols) and simulated (solid lines) harmonic output for the (a) SiC MESFET and (b) GaN HEMT doublers.

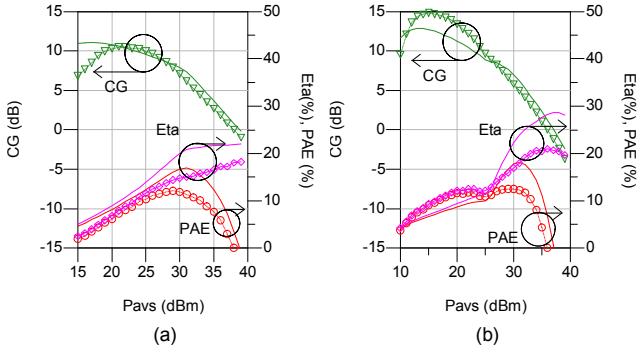

Fig. 7. Measured (symbols) and simulated (solid lines) CG, η and PAE for the (a) SiC MESFET and (b) GaN HEMT doublers.

The output powers of the SiC MESFET and GaN HEMT doublers were assessed over a 5% fractional bandwidth around f_o and the characteristics are provided in Fig. 8a and 8b, respectively. The SiC MESFET doubler is measured at an available power of +36dBm while the GaN HEMT doubler is measured at an available power of +33dBm. Simulations of the high power doublers are extremely close for the first and second harmonics. For the SiC MESFET doubler, the third harmonic falls 51.49dB below the second at the center frequency and consequently is more difficult to predict over a frequency range of interest. The 3dB bandwidths of the SiC MESFET and GaN HEMT doublers are 4.2% and 4.0%, respectively, due to the narrowband nature of the realized networks.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

Work	2fo (GHz)	CG (dB)	Pout (dBm)	(%)	PAE (%)	fo / 3fo at sat. Pout (-dBc)
SiC*	4	10.00	38.00	18.16	12.03	-39.5/-52.66
GaN*	6.66	14.80	36.17	20.95	12.47	-36.45/-26.17
[2]	8	3.00	25.00	—	—	-11/-27
[4]	2.4	11.18	21.85	—	—	—/—
[5]	28-30	18.00	22.00	—	—	-50 to -70/-60
[6]	30	16.00	18.00	5.00	—	-23/—
[7]	10	11.67	10.34	—	—	-7/-23

*This work

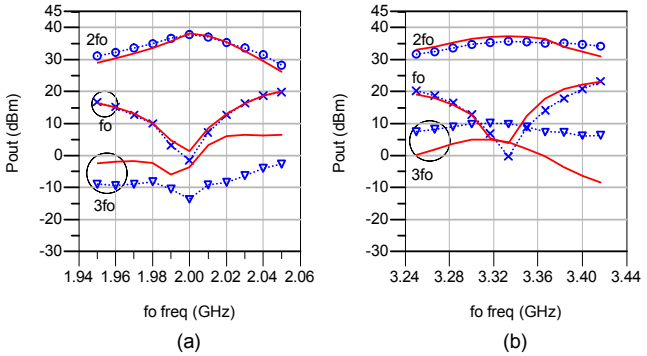

Fig. 8. Measured (symbols) and simulated (solid lines) harmonic output power over a 5% BW for the (a) SiC MESFET and (b) GaN HEMT doublers.

V. CONCLUSION

High power, high conversion gain frequency doublers employing silicon-carbide MESFET and gallium nitride HEMT devices have been developed using harmonic load- and source-pull simulations performed utilizing precision nonlinear device models. These models have been shown to closely predict the performance of the measured realized doublers. The performance demonstrated by this work appears to provide the highest frequency doubled output power reported for single-ended active frequency doublers.

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