Highly Efficient Operation Modes in GaN Power Transistors Delivering Upwards of 81% Efficiency and 12W Output Power

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***Abstract* — This paper investigates the development of an inverse class-F design procedure for obtaining very high efficiency performance at high power levels. RF waveform engineering was used to obtain high efficiency inverse class-F waveforms at the device current-generator plane. Drain efficiencies above 81% have been achieved at 0.9 and 2.1GHz for a wide band-gap gallium nitride (GaN) HEMT transistor and 12W fundamental output power. Investigations into improvements in drain efficiency through increases in drain bias voltage have yielded drain efficiencies of up to 84% at 2.1GHz. To the author's knowledge, the efficiencies presented in this study are the highest published, measured efficiencies of a high power GaN HEMT at these frequencies.**

***Index Terms* — MODFETs, power amplifiers.**

I. Introduction

High power, high efficiency amplifiers are of great importance in the current climate of energy conservation which demands high efficiency communication systems. A previous inverse class-F design study has shown that higher theoretical efficiencies can be obtained compared to class-F amplifiers when considering 'on-resistance' effects [1]. The large voltage swing associated with inverse class-F operation, that is key to the high power and high efficiencies achievable in this mode of operation, can often be difficult to realise with many current device technologies (e.g. LDMOS, GaAs) due to the limitations induced by device breakdown voltages.

However, with advancements in wide band-gap semiconductor technologies (GaN, SiC), large rail voltages become feasible, hence allowing for power amplifiers with very high efficiency performance to be realised. For the case of the device output power being held constant, an additional advantage arises in that the maximum drain current swing can be reduced to minimise any knee-walkout effect [2-3].

In this study a 10W GaN HEMT was used. Measurements were carried out at two fundamental frequencies of 0.9GHz and 2.1GHz (two of the major communication frequencies) using the active harmonic load-pull waveform measurement system developed at Cardiff University [4]. A procedure developed for optimising class-F operation for on-wafer devices in [5] has been adapted in the development of an inverse class-F design procedure for optimising efficiency of packaged high power devices. The implemented de-embedding process [6] allows for analysis and engineering of the RF waveforms that exist at the device current-generator plane ($I_{gen.}$-plane).

II. Package Parasitic Modeling & De-embedding

Generating an equivalent circuit model for the parasitic effects of the device package allows predictions for the required open and short terminations at the package-plane to be made. The utilised TRL calibration generates a measurement reference-plane at the device package and not, as is the case for on-wafer measurements, close to the device $I_{gen.}$-plane. Thus, the approximated package network provides a means of predicting and analysing operation at the $I_{gen.}$-plane during the design process. This process is essential for enabling RF waveform engineering as it allows for correlation between the measured dynamic I-Vs and the device DCIV plane, which defines the boundaries of the device performance.

The complex loads at the package-plane can be calculated from ideal load values through S-parameter simulations of the parasitic model. Table-I presents the reflection coefficients required, at both the current generator and package reference planes, to establish inverse class-F operation, whilst operating at a drain voltage of 28V at 0.9GHz and also for 2.1GHz.

Frequency	$I_{gen.}$-Plane	Package-Plane 0.9GHz	Package-Plane 2.1GHz
f_0	$0.13 \angle 0°$	$0.26 \angle 82°$	$0.47 \angle 126°$
$2f_0$	$\mathbf{1} \angle 0°$	$1 \angle 99°$	$1 \angle 169°$
$3f_0$	$1 \angle 180°$	$1 \angle -145°$	$1 \angle -72°$

Table-I. Inverse class-F terminations at current generator & package planes for 28V drain voltage at 0.9GHz and 2.1GHz.

III. GaN HEMT in Inverse Class-F Mode

A. Inverse Class-F Theoretical Efficiencies

The ideal inverse class-F output waveforms of half-wave rectified voltage and square current represent a perfectly functioning, 100% efficient inverse class-F amplifier. In reality this ideal performance is compromised by DC offsets, as well as the ability to generate the perfect harmonic terminations required. Assuming terminations up to the fifth harmonic in the current waveform (through

hitting the current boundary conditions), and up to the second harmonic in the voltage waveform (through active harmonic load pull waveform engineering), a bandwidth limitation factor is applicable to the ideal drain efficiency [1,7]. Using the equation for drain efficiency (η_{drain}) in [1], the theoretical efficiency for a three-harmonically controlled inverse class-F amplifier design with offset, V_{knee}, becomes that shown in Eq. 2.

$$\eta_{voltage} \cdot \eta_{current} = 1.000 \times 0.854 = 0.854 \qquad (1)$$

$$\eta_{drain} = 100 \times \frac{V_{DC} - V_{knee}}{V_{DC}} \times 0.854 \qquad (2)$$

B. Initial gate bias sweeps at 0.9GHz

Processes implemented in [5] for obtaining highly efficient class-F designs were adapted in order to begin developing a procedure for obtaining an optimised inverse class-F design. This included a sweep of gate bias voltage to identify an optimum bias point which was conducted with the necessary fundamental and harmonic terminations, as stated in Table-I, in place. The drive level during the sweep was such that output compression was approximately -3dB.

Once package-plane measurements were obtained the equivalent circuit model for the output parasitics and device package was utilised to de-embed to, and reveal, the $I_{gen.}$-plane current and voltage waveforms [6]. It was then possible to select a gate voltage which would allow a squared output current and half-rectified output voltage waveform to be obtained. To achieve this, both the ratio of the second harmonic voltage to the fundamental voltage, and the ratio of the third harmonic current to the fundamental current, was selected in accordance with inverse class-F theory. Due to the limited number of harmonic terminations employed, the optimum harmonic current and voltage ratios required were less than those for the ideal design; approximately 0.18 and 0.29 respectively.

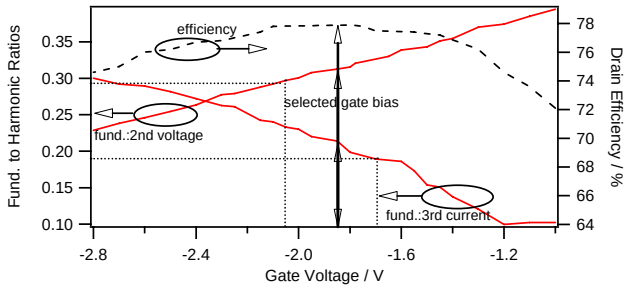

Fig. 1. Gate sweep at 28V drain voltage bias condition at 0.9GHz.

Tradeoffs between both of these ratios were necessary as the required voltage and current ratios did not occur at the same point in the gate voltage sweep. Therefore, at 0.9GHz, the final gate bias of -1.85V was selected at the efficiency peak, as shown in Fig. 1.

C. Optimisation of load impedances and results at 0.9GHz

Following the selection of the gate bias, the predicted load impedances in Table-I were optimised. In a first step the fundamental load impedance at the I_{gen}-plane was swept between 60Ω and 70Ω. Once the optimum for the fundamental impedance was determined the phase of the second harmonic was swept by ±10° of the figure in Table-I to compensate for any small errors in the approximated package model. The same sweep was then applied to the third harmonic phase. The resulting optimised impedance values at the I_{gen}-plane are given in Table-II.

Frequency	$I_{gen.}$-Plane	Package-Plane
f_0	0.14 ∠ 0°	0.27 ∠ 86°
$2f_0$	1 ∠ -6°	**1** ∠ 91°
$3f_0$	1 ∠ -174°	1∠ -142°

Table-II. Optimum terminations for Vds=28V at 0.9GHz.

A power sweep was conducted with the optimised gate bias, fundamental load and harmonic impedances. The results at 0.9GHz are shown in Fig. 2. The maximum efficiency achieved was 81.5%, at a gain compression of 4.5dB and 40.9dBm fundamental output power.

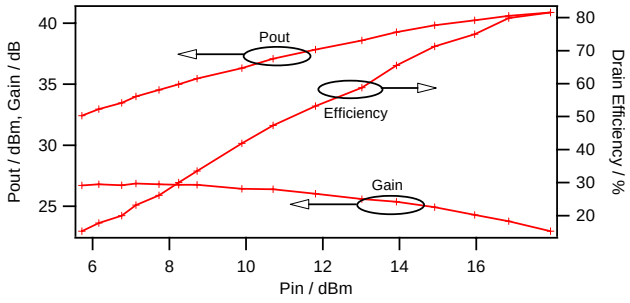

Fig. 2. Power sweep at 28V drain voltage bias condition at 0.9GHz.

All waveforms measured were imported into Agilent's ADS simulation environment and, were de-embedded to the current generator plane using the previously discussed package parasitic model. Fig. 3 shows the de-embedded output current and voltage waveforms obtained at the drive level delivering maximum efficiency of 81.5%. Fig. 4 shows the comparison between the package-plane and de-embedded $I_{gen.}$-plane RF load lines.

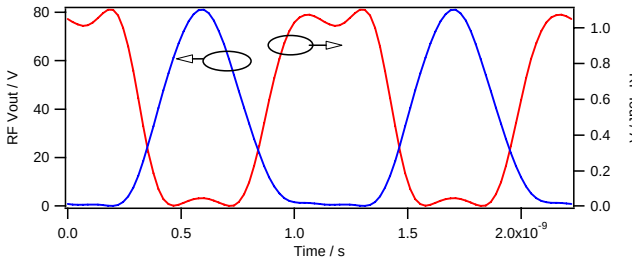

Fig. 3. Measured 81.5% efficient RF waveforms, de-embedded to the $I_{gen.}$-plane at Vds=28V and 0.9GHz.

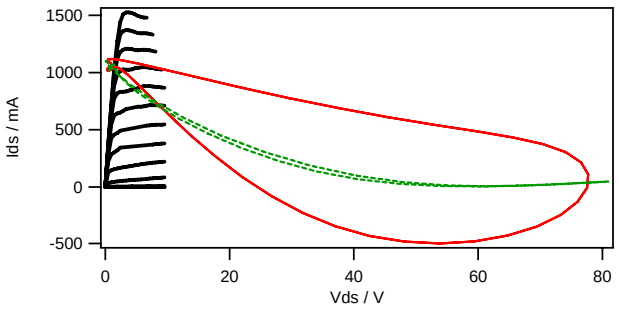

Fig. 4. Measured package-plane RF load-line (solid) and de-embedded RF load-line (dotted) at Vds=28V, 81.5% efficiency.

In conclusion, the waveforms in Figs. 3 and 4 not only show that high efficiency inverse class-F operation has been achieved at 0.9GHz, but also that the package model has been verified as accurate at least up to 2.7GHz through de-embedding of the waveforms to the $I_{gen.}$-plane.

IV. Design Towards High Efficiency at 2.1GHz

A. Inverse class-F scaled to 2.1GHz at 28V

With the successful waveform optimisation for inverse class-F at 0.9GHz completed, performance scalability to higher frequencies was investigated. For this purpose the gate bias sweep was repeated at 2.1GHz, this time delivering an optimum of V_{gs}=-2.5V.

However, by applying the predicted load impedances in Table-I for 2.1GHz, and performing a power sweep, it was found that a disappointing 69.3% drain efficiency was obtained with 40.9dBm fundamental output power at 28V drain voltage. To gain a further optimised performance, the phases of the harmonic loads were now swept across a wider range of angle than the previous ±10°, with the aim of obtaining an optimum efficient mode of operation. Following the optimisation of the harmonic impedances a high density sweep of the fundamental load was conducted resulting in an optimised $I_{gen.}$-plane load with a more substantial complex offset. The final optimised package-plane and de-embedded harmonic loads are listed in Table-III for a drain voltage bias condition of 28V. Utilising these values a power sweep with a 28V drain voltage was conducted, with the results display in Fig. 5 indicating a maximum drain efficiency of 82.3%.

B. Inverse class-F scaled up to V_{ds} of 40V

The high voltage breakdown nature of the wide band-gap GaN device technology proves ideal in securing the very high voltage swings required for high power inverse class-F operation. This combined with the very low knee voltage, inherent with this GaN HEMT device technology, offers the possibility of reaching very high levels of drain efficiency whilst operating at these high power levels.

With the design procedure scaled to 2.1GHz an investigation was made on its scalability towards higher drain bias voltages. For this purpose the drain bias voltage was increased above 28V to 35 and 40V, respectively.

The same GaN HEMT device was used with output power and compression kept approximately constant for each of the DC drain voltage levels. As DC drain voltage was increased, an appropriate reduction of the output current swing as a result of the increased voltage swing was therefore required. During the scaling of the drain voltage the same gate bias of V_{gs}=-2.5V and harmonic load impedances, according to Table-III, were maintained.

The obtained results at a 35V drain voltage bias condition saw the drain efficiency improve up to 82.8% whilst with a 40V bias condition 84.0% drain efficiency was measured.

Frequency	$I_{gen.}$-Plane	Package-Plane
f_0	0.14 ∠ 39◦	0.52 ∠ 129°
$2f_0$	1 ∠ -75°	**1** ∠ 129°
$3f_0$	1 ∠ -170°	1∠ -69°

Table-III. Optimum terminations for Vds=28V at 2.1GHz.

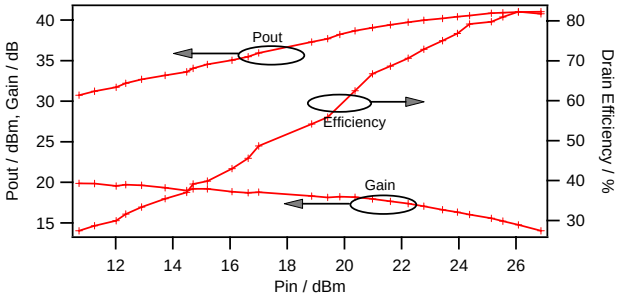

Fig. 5. Power sweep at 28V drain voltage bias condition at 2.1GHz

V. Waveforms & Performance Analysis

Fig. 6 shows the de-embedded output current and voltage waveforms present at the I_{gen}-plane at maximum drain efficiency of 82.3% at V_{ds}=28V. As can be seen, with decreasing current swing the de-embedded current and voltage waveforms were beginning to extend beyond the defined DCIV boundaries of the device. This was due to the inaccuracies in the package model becoming more apparent at the higher harmonic operating frequencies, as well as the increased effects from the weakly non-linear output capacitance. Nevertheless, these de-embedded waveforms are still effectively indicating the performance of the device at the $I_{gen.}$-plane. As can be seen from Fig. 6, the de-embedded voltage waveform maintains the half-rectified sinusoid indicative of inverse class-F. However, squaring of the current waveform is also indicated in the de-embedded output current waveform, but to a lesser extent. The same measurements and analysis were made for the 35V and 40V drain voltage conditions showing almost ideal voltage waveforms, but continuously diverging current waveforms away from the ideal.

This can be explained by errors within the de-embedding package and parasitic model which become more critical at higher frequencies. However, the accuracy of the de-embedded waveforms at 0.9GHz does seem to suggest that the linear part of the package and parasitic model is accurate. It is therefore thought that the distortion in the output current is introduced by the slight non-linearity of the device output capacitance, C_{ds}, having an increasing effect towards higher freqencies. This is supported by the observed increase in current distortion as V_{ds} increases.

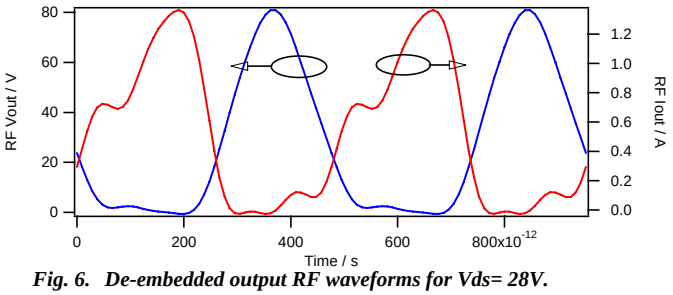

Fig. 6. De-embedded output RF waveforms for Vds= 28V.

It is also interesting to note that the maximum incurred voltages at the $I_{gen.}$-plane did scale very well with increasing rail voltages. The maximum incurred output voltages ($V_{max.}$) for the 28V, 35V and 40V drain bias conditions are 82V, 102V and 121V respectively, and very closely replicate the theoretical values for inverse class-F obtained from Eq. 3 below.

$$V_{\max.} = \pi \cdot (V_{DC} - V_{knee}) \qquad (3)$$

Fig. 7 shows a comparison between the measured and theoretical relationship between the maximum measured RF output voltage and the DC drain voltage bias condition. The measured relationship shows a good conformance to that calculated using Eq. 3. The voltage offset, of approximately 3V observable at each drain bias voltage, can be accounted for by the smaller fundamental-to-second-harmonic voltage ratio being implemented due to trade-offs in the gate bias voltage chosen. Conclusively, the utilised GaN technologies did not indicate any onset of RF breakdown up to 121V.

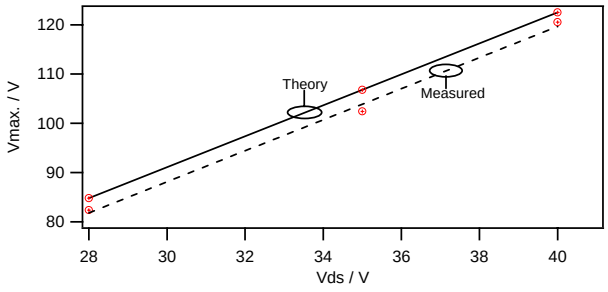

Fig. 7. Measured and theoretical peak output voltage at $I_{gen.}$-plane.

Furthermore, the very high efficiencies obtained in this study are achieved at a high extent of gain compression of the device (between 4 to 5dB compression). It is important to stress, that even under such high state of compression, this device continues to operate very efficiently and at gain levels of 14dB and above. Consequently, PAE is lower only by 0.5 to 3.5% compared to drain efficiency across all optimised efficiency conditions detailed in this research. The high gain of this GaN device lends itself very well to this high efficiency application.

VI. Conclusion & Discussion

The procedures described in this paper, to obtain very high efficiency performance from a GaN HEMT, show a systematic methodology in which maximum achievable practical efficiencies of an inverse class-F amplifier topology are obtained and analysed at 0.9GHz. At 2.1GHz the uncontrolled measurement system harmonic impedances conspire to prevent inverse class-F operation from being achieved, and instead another high efficiency mode is obtained. This performance was shown and verified through the combination of high-power waveform measurements and device package de-embedding, whilst also analysing how increased DC drain bias voltage can lead to further improved record efficiencies, and the output voltage scaling as defined in the half rectification of the output voltage waveform.

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References

[1] Y. Y. Woo, Y. Yang and B. Kim, "Analysis and Experiments for High-Efficiency Class-F and Inverse Class-F Power Amplifiers," *IEEE Trans. Microwave Theory & Tech.*, vol. 54, no. 5, pp. 1969-1974, May 2006.

[2] Chris Roff, et al., "Detailed Analysis of DC-RF Dispersion in AlGaN/GaN HFETs using Waveform Measurements," *European Microwave Integrated Circuits Conference, 2006. The 1st* , vol., no., pp.43-45, Sept. 2006.

[3] J. Lees, et al., "Experimental gallium nitride microwave Doherty amplifier," *IEEE Electronic Letters*, pp. 1284-1285, November 2005.

[4] J. Benedikt et al., "High Power Time Domain Measurement System with Active Harmonic Load-pull for High Efficiency Base Station Amplifier Design," *IEEE MTT-S Int. Microwave Symp.* Digest, pp. 1459-1462, June 2000.

[5] C. Roff, J. Benedikt and P. J. Tasker, "Design Approach for Realization of Very High Efficiency Power Amplifiers," *2007 IEEE MTT-S Int. Microwave Symp. Digest*, pp. 143-146, June 2007.

[6] A. Sheikh et al., "The Impact of System Impedance on the Characterization of High Power Devices," Proceedings of the 37th European Microwave Conference, pp. 949-952, Oct 2007.

[7] Raab, F.H., "Maximum efficiency and output of class-F power amplifiers," *Microwave Theory and Techniques, IEEE Transactions on* , vol.49, no.6, pp.1162-1166, Jun 2001.