High-power, High-efficiency Power Amplifier Reference Design in III-V Wide Bandgap Gallium Nitride Technology using Nonlinear Vector Network Analyzer and X-parameters

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***Abstract* — This paper presents a complete power amplifier design using new Nonlinear Vector Network Analyzer (NVNA) and X-parameter technologies. A high-power, pulsed Continuous Wave (CW) NVNA setup is presented and harmonic tuning capabilities of the measured X-parameter model is demonstrated using the same setup. From fundamental and harmonic impedance tuning, input and output power amplifier matching networks are synthesized and first-pass design success is confirmed by measurements of the fabricated power amplifier.**

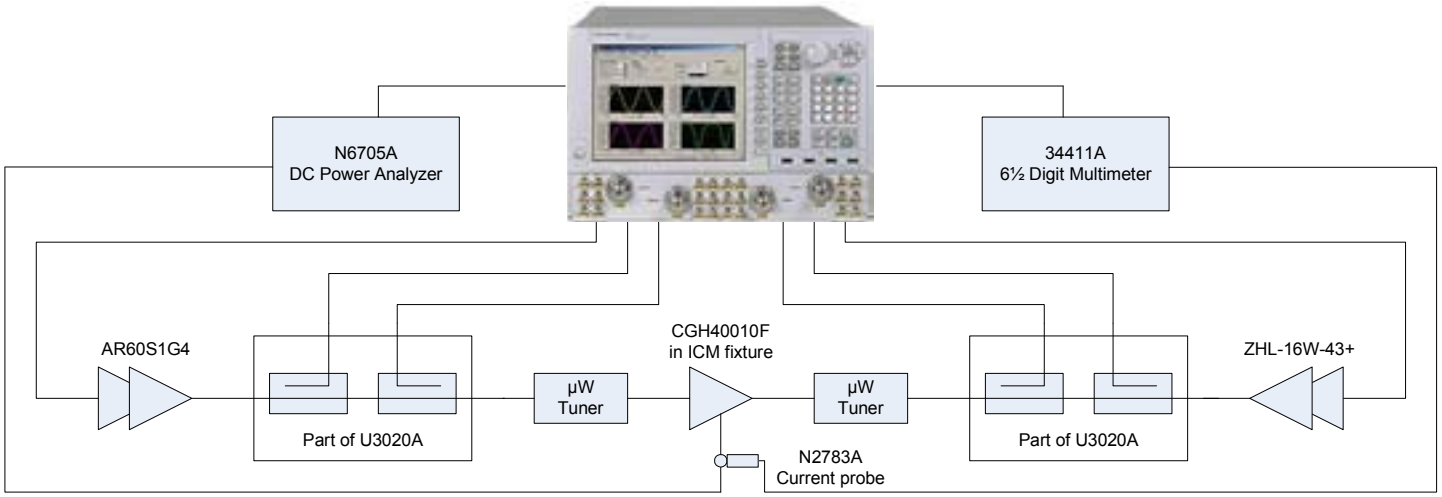
***Index Terms* — Nonlinear vector network analyzer, X-parameters, behavioral modeling, power amplifier design, gallium nitride, high power, high efficiency.**

I. Introduction

Compact transistor models currently available for wide bandgap III-V technologies such as Gallium Nitride (GaN) generally suffer from long development times and limited accuracy [1]. Inaccuracies are largely attributed to details in the device physics that may not yet be fully known or accurately implemented into the underlying model framework. Using NVNA data, however, there have been significant recent advances [2]. And, also based on NVNA, X-parameters have recently been demonstrated as a powerful behavioral level modeling approach with appealing device model properties [3, 4]. Contrary to compact models, this type of model assumes no *a priori* knowledge of the internal device composition. Instead, it relies exclusively on wisely selected large-signal measurements and mathematical fitting functions, which may approximate device transfer characteristics very accurately [5]. In this paper, it is demonstrated how nonlinear VNA and X-parameters are used to bridge the gap currently found between GaN transistor physics and simulator models in a complete power amplifier design developed entirely inside the circuit simulator, but based on measured nonlinear data. Section II outlines the details of the hardware setup used to measure X-parameters of a commercially available GaN power transistor. Section III describes the amplifier design developed in the circuit simulator. Section IV compares results from the circuit simulator to measurement results of the fabricated PA.

II. Pulsed CW X-parameter Measurements using NVNA

In this work, an unmatched 10W High Electron Mobility Transistor (HEMT) is used (CGH40010F from CREE). The power transistor is biased in deep Class AB operation and the hardware setup used to characterize the transistor and extract its X-parameters is shown in Fig. 1. Essential to this setup is the N5242A 10MHz to 26.5GHz 4 port PNA-X with two phase comb generators (U9391C) for cross-frequency phase calibration and measurement. The following NVNA firmware capabilities are installed on the instrument: Option 510 (Base NVNA firmware), Option 514 (X-parameters), and Option 520 (Load-dependent X-parameter extension). The PNA-X/NVNA controls all hardware in the setup as well as the complete X-parameter measurement sequence.



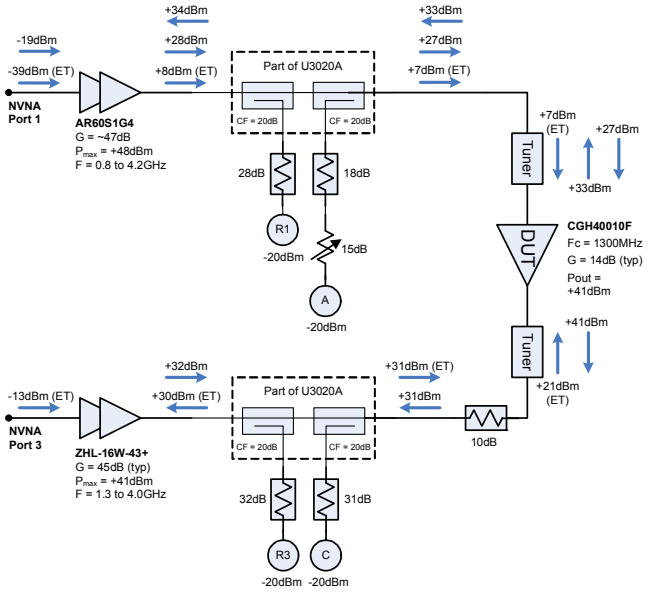


Fig. 2. NVNA power budget is calculated based on DUT specifications and the PNA-X receiver linearity requirements.

As the CGH40010F is packaged, a microwave transistor test fixture is used to establish measurement reference planes directly at the transistor gate and drain terminals from an in-fixture TRL calibration. All measurements are performed under pulsed Continuous Wave (CW) conditions using a 1.3GHz carrier frequency with 100µS pulse width and 10% duty cycle. Pulse generators and pulse modulators internal to the PNA-X are used to control the RF pulse conditions [6]. Standard PNA-X input power ratings are typically +30dBm at the test ports (or +40dBm with Option H85). Thus, to accommodate DUT power levels, a high-power NVNA test set (U3020A) is employed and adequate power levels for input drive and X-parameter output measurements are provided by two linear bench amplifiers (AR60S1G4 and ZHL-16W-43+, respectively). To sustain measurement receiver linearity requirements (-20dBm at receivers at peak powers), the NVNA power budget is calculated from DUT specifications and sufficient attenuation is added at receiver inputs (Fig. 2).

The measurement setup is also equipped with fundamental mechanical tuners to extend the measured X-parameter model into highly mismatched source and load conditions [7]. Tuner control software is installed directly on the PNA-X platform. Two N6705A DC power analyzer modules are used for device gate and drain DC biasing. Bias conditions are automatically embedded into the measured X-parameter model. Large Electrolytic Capacitors (ELCOs) placed at the transistor fixture combined with lead wire inductance to the fixture drain terminal prevent accurate current measurements using the N6705A DC power analyzer. Instead, an N2783A current probe placed between transistor drain terminal and the ELCOs takes several in-pulse current samples. Samples are then averaged by the NVNA to ensure very accurate Power Added Efficiency (PAE) measurements.

A. Calibration

The NVNA calibration includes three steps: Vector calibration, phase calibration, and amplitude calibration. NVNA calibration reference planes are defined at the tuner APC7 coaxial connectors. The TRL based fixture files are then used to de-embed measurements to the device gate and drain terminals. Phase calibration establishes a harmonic phase reference signal with a constant phase relationship versus frequency. Incident and reflected waves are ratioed against this signal to eliminate arbitrary phase shifts introduced when sweeping the PNA-X local oscillator. Amplitude calibration corrects the receivers using a power meter at one of the tuners. To avoid damage to the calibration standards, it may be advantageous to calibrate the system after removing preamplifiers or increasing source attenuation. Changing preamplifiers or attenuators between the RF source and reference coupler, does not affect measurement accuracy as the NVNA uses 8-term error vector correction.

B. X-parameter Model Validation

An essential step in the development of any simulation model is validation. The extracted load-dependent X-parameter model is validated in multiple ways. First, it is checked against DC and small-signal S-parameter measurements over the range of bias conditions. Then, it is checked against large-signal measurements both at load conditions included in the extraction data (to verify that the model plays-back large-signal measurements correctly) and at independent load conditions not used during model extraction (to validate interpolation capabilities within the measured load grid). Example validation results are presented in Fig 3-4.

Although the measurement setup depicted in Fig. 1 employs fundamental tuners only, the X-parameter framework contains, in addition to the large-signal AM/AM and AM/PM transfer functions, also small-signal *S* and *T* terms providing harmonic load sensitivities of the DUT behavior at input and output ports [2]. These are derived from phase-swept active source-

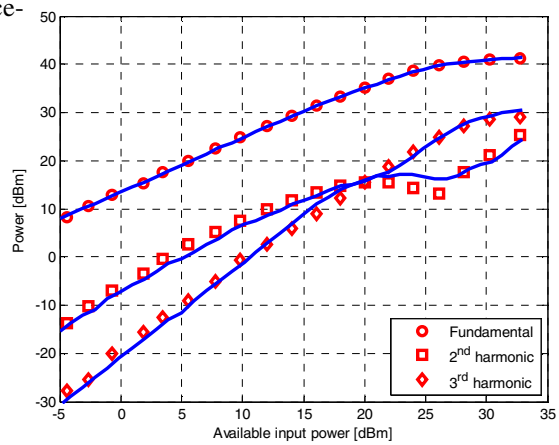


Fig. 3. Simulated (blue) and measured (red) fundamental and harmonic power at R_L=29.5+j19.5ohm (not used in extraction data).

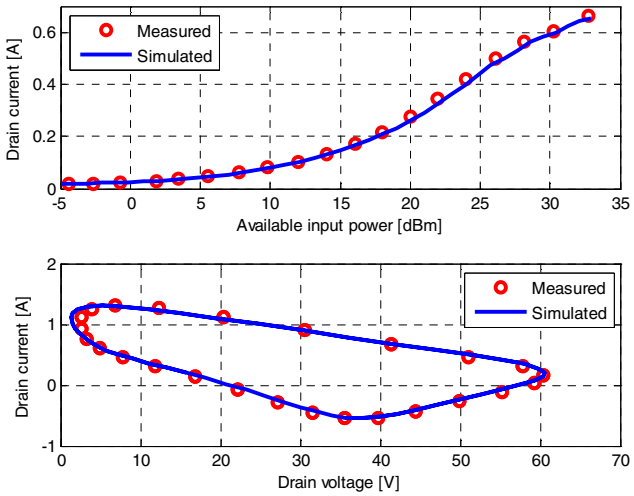


Fig. 4. *Upper:* Simulated (blue) and measured (red) device drain current at a fundamental load of 20.1+j26.5ohm. *Lower:* Simulated (blue) and measured (red) dynamic load lines at a fundamental load of 20.1+j26.5ohm and at +20dBm available input power.

and load-pull measurements and scope out impedance regions around fundamental and harmonic terminations where models can be accurately source- and load-pulled. The effect of *S* and *T* terms is readily recognized from comparison between simulated and measured fundamental load-pull results (Fig. 5, black and red contours, respectively). In a fundamental load-pull setup with mechanical tuners like the one in Fig. 1, tuning at the harmonic frequencies is uncontrolled. The slugs used in slide-screw tuners are typically very wideband, but the reflection phase is rotated along the tuner slabline and highly offset at harmonic frequencies (Fig. 6). Due to the X-parameter *S* and *T* terms, harmonic impedances must be properly embedded in the simulator to accurately reproduce measured load-pull results (Fig. 5, blue contours). In an amplifier design, purpose of the matching network is not only to provide a certain load line at the fundamental frequency.

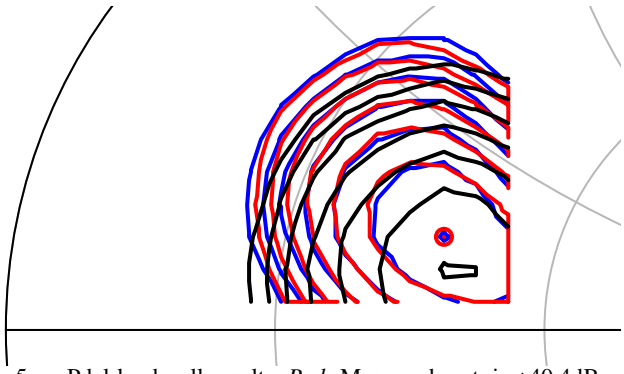


Fig. 5. Pdel load-pull results. *Red:* Measured, opt. is +40.4dBm at 33+j12ohm; *Black:* Simulated with fundamental load tuner impedances only, opt. is +40.3dBm at 38+j9ohm; *Blue:* Simulated with fundamental, 2nd and 3rd harmonic tuner impedances, opt. is at +40.4dBm at 33+j12ohm.

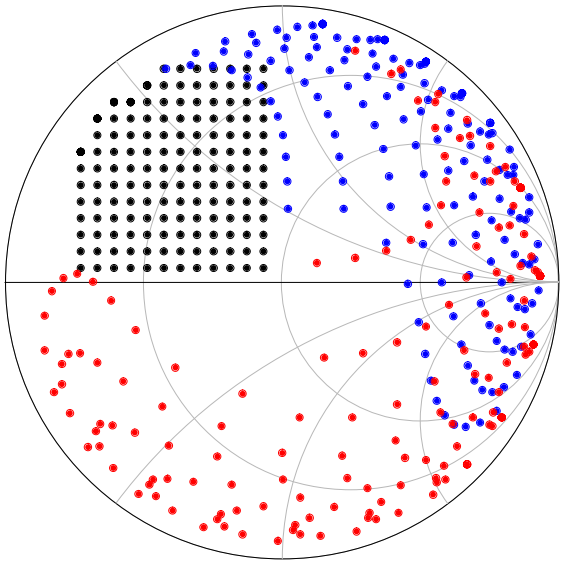


Fig. 6. Measured loads presented to the DUT. *Black:* Fundamental loads. *Blue:* 2nd harmonic loads. *Red:* 3rd harmonic loads.

Higher order harmonic content, especially in the device output, plays also a major role. The harmonic tuning capabilities demonstrated in Fig. 5 are thus very essential [4].

III. Power Amplifier Design using X-parameters

In a deep Class AB operation, harmonic power at the output Z_0 is generally unwanted and should either be shorted or reflected back to the device with proper phase angle. Several matching topologies may fulfill such requirements. Here, we employ lowpass filter structures realized using microstrip elements on a high quality Rogers Duroid 6010 laminate.

A. Output Match

Design objectives are to maximize output power and efficiency while also minimizing harmonic content at the output Z_0 (i.e., optimizing amplifier linearity). The chosen output match topology is depicted in Fig. 7 (upper). Albeit the filter structure should be designed in low Q circles, the impact on harmonics was also carefully considered. For optimum 3rd harmonic suppression, the open stub (osc3) is designed with an electrical length equal to a short at $3F_c$. Fig. 7 (lower) shows the idealized element transformation within a constant 0.6 Q_n circle. A final transformation to the drain terminal is done using a DC feed with an 80 degrees electrical short at $2F_c$.

B. Input Match

The purpose of the input matching network is to transform source Z_0 to a proper gate impedance that yields optimum power gain and stability. At lower frequencies, the CGH40010F has higher gain and is prone to oscillate. For frequency octaves lower than F_c, a series resistor is thus added to limit the source reflection coefficient. The DC gate bias

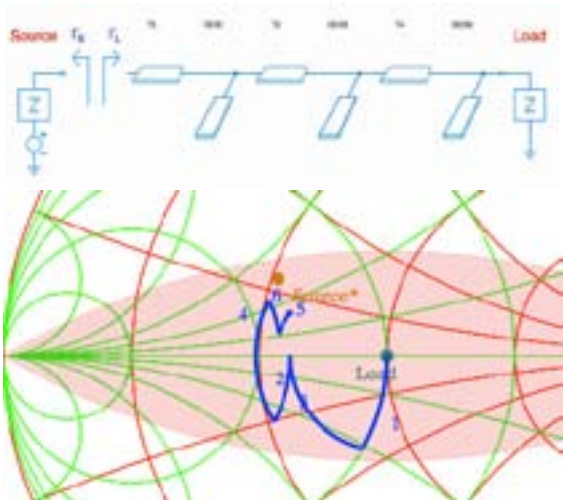


Fig. 7. *Upper:* Simplified output match topology. *Lower:* Idealized transformation within a constant Q_n circle of 0.6 (shaded area).

feed is constructed using a high impedance meander quarter wavelength transformer with degraded Q to lower the reflection circle at the 2nd harmonic.

IV. Results

The fabricated PA is shown in Fig. 8. Simulated and measured amplifier AM/AM and drain efficiency vs. delivered output power is shown in Fig. 9. Measured saturated output power is +41.9dBm (simulation predicts +42.1dBm) and measured max. drain efficiency is 66.6% (simulation predicts 66.7%). Overall simulation and measurement results agree very well.

V. Conclusions

In this paper, it has been demonstrated how an unmatched 10W GaN HEMT power transistor can be characterized and modeled using NVNA and X-parameters. From measured X-parameters, a complete high-power, high-efficiency deep class

Fig. 8. The fabricated PA mounted on an aluminum heat sink.

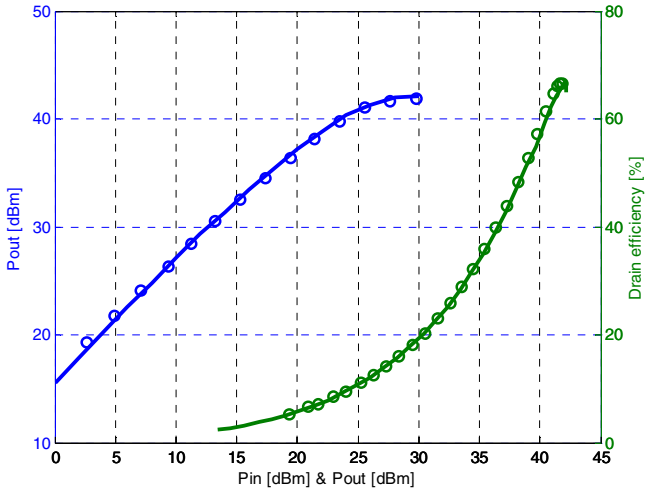


Fig. 9. Simulated (solid) and measured (dotted) AM/AM (blue) and drain efficiency (green) power amplifier characteristics.

AB power amplifier was designed in the circuit simulator. Measurements of the fabricated amplifier confirm a first-pass design success with less than 0.2dB and 0.3% overall deviation between simulated and measured amplifier AM/AM and drain efficiency characteristics, respectively.

Acknowledgement

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