

A High-Efficiency 100-W Four-Stage Doherty GaN HEMT Power Amplifier Module for WCDMA Systems

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Abstract — In this paper, a novel high-efficiency four-stage Doherty power amplifier architecture convenient for practical implementation in base station applications for modern communication standards has been proposed and fabricated. In practical verification, each power amplifier is based on a 25-W Cree GaN HEMT device with the transmission-line load network corresponding to an inverse Class F mode approximation. In a CW operation mode with the same bias voltage for each transistor, an output power of 50 dBm with a drain efficiency of 77% was achieved at a supply voltage of 34 V. In a single-carrier WCDMA operation mode with PAR of 6.5 dB, a high drain efficiency of 61% was achieved at an average output power of 43 dBm, with $ACLR_1$ measured at -31 dBc level.

INTRODUCTION

In modern wireless communication systems such as CDMA2000, WCDMA, or OFDM with increased bandwidth and high data rate, the transmit signal is characterized by a high peak-to-average power ratio (PAR) due to wide and rapid variations of the instantaneous transmit power. As a result, power-amplifier enhancement techniques to improve efficiency and linearity simultaneously have become critical. To increase efficiency of the power amplifier, it is possible to apply a switching-mode inverse Class F mode technique [1, 2]. However, this kind of a power amplifier requires an operation in saturation mode resulting in a poor linearity, and therefore is not suitable to directly replace linear power amplifiers. However, to obtain high efficiency and good linearity simultaneously, such kind of nonlinear high-efficiency power amplifier operating in an inverse Class F mode can be used in advanced Doherty transmitter architectures with digital feedback predistortion linearization technique [3, 4]. The innovative high-efficiency four-stage Doherty amplifier architecture presented in this paper is based on four identical 25-W GaN HEMT power amplifiers configured in an inverse Class F mode and designed to provide a highly efficient operation in a frequency bandwidth of 2.11 to 2.17 GHz with a drain efficiency over 60% at a single-channel WCDMA output power of 20 W with an adjacent channel leakage power ratio of better than -30 dBc without linearization loop.

ARCHITECTURES

An conventional two-way asymmetric Doherty architecture exhibits a significant drop in efficiency in the region between the efficiency peaking points, especially for large power ratios between the carrier and peaking amplifiers [5]. However, it is possible to use more than two power amplifiers in order to prevent significant deterioration of efficiency at backoff output power levels. This can be provided by the so-called multistage Doherty amplifiers, the operation of which is analogous to that of the conventional two-stage Doherty amplifier. The basic multistage Doherty power amplifier architecture shown in Fig. 1(a) uses more than one peaking amplifier, with quarterwave transmission lines to combine their output powers [6]. The characteristic impedances of each output quarterwave transmission line depend on the levels of backoff power and can be calculated from

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$$Z_{0i} = R_L \prod_{j=1}^i \gamma_j \quad (1)$$

$$\prod_{j=k}^{(i+k)/2} \gamma_{(2j-k)} = 10^{(B_i/20)} \quad (2)$$

where $i = 1, 2, \dots, N - 1$, $k = 1$ (for odd i) or 2 (for even i), N is the total number of amplifier stages, and B_i is the backoff level (positive value in decibels) from the maximum output power of the system, at which the efficiency peaks. The maximum level of backoff B_{N-1} is set by the carrier amplifier while the number of efficiency peaking points is directly proportional to the number of amplifier stages used in the design.

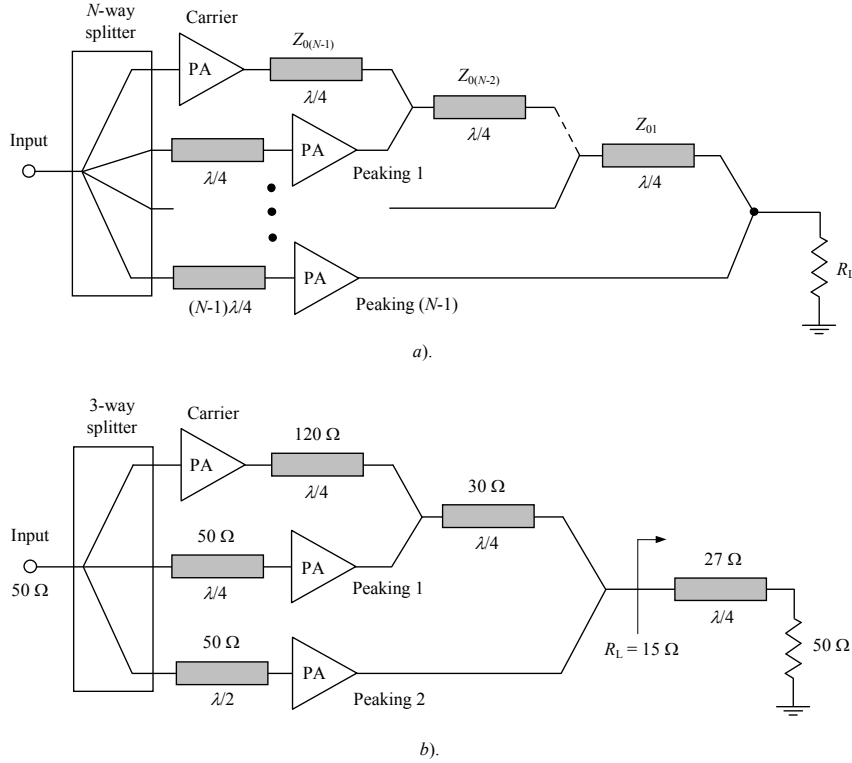


Fig. 1. Multistage Doherty amplifier architectures.

Figure 2 shows the instantaneous drain efficiencies of the multistage Doherty power amplifier architectures for two, three, and four stages, having maximum efficiencies at the transition points of -6 dB, -12 dB, and -18 dB backoff output power levels, respectively. From Fig. 2 it follows that the multistage architecture provides higher efficiencies at backoff levels in between the efficiency peaking points compared with asymmetric Doherty architecture and significantly higher efficiency at all backoff output power levels compared with the conventional Class B power amplifiers. For the most practical case of a three-stage Doherty power amplifier whose block schematic is shown in Fig. 1(b), the characteristic impedances of each output quarterwave transmission line can be obtained from Eqs. (1) and (2) to be

$$Z_{01} = \gamma_1 R_L \quad (3)$$

$$Z_{02} = \gamma_1 \gamma_2 R_L \quad (4)$$

where

$$\gamma_1 = 10^{(B_1/20)} \quad (5)$$

$$\gamma_2 = 10^{(B_2/20)} \quad (6)$$

where $B_1 = 6$ and $B_2 = 12$ dB for peak efficiencies at -6 dB and -12 dB backoff points, respectively, resulting in $Z_{01} = 30 \Omega$ and $Z_{02} = 120 \Omega$ for $R_L = 15 \Omega$.

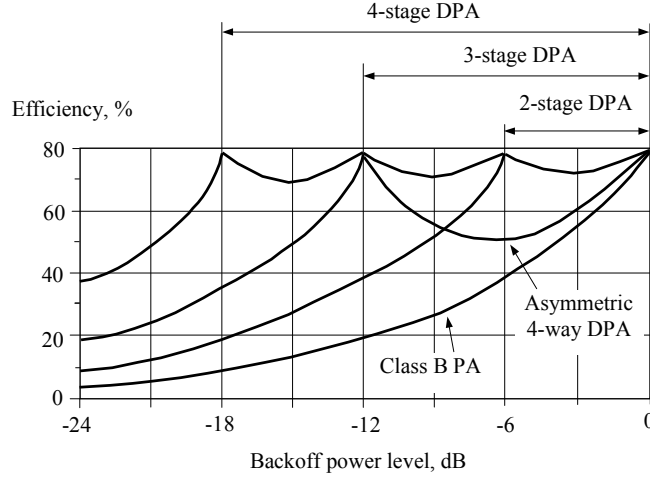


Fig. 2. Efficiencies of the different Doherty amplifier architectures.

For a 1.95-GHz WCDMA application, a three-stage Doherty power amplifier structure using GaAs FET devices with the device periphery ratio of 1:2:4 and microstrip power combining elements provides a *PAE* of 48.5% and a power gain of 12 dB at $P_{1dB} = 33$ dBm. The peak power-added efficiencies of 42% and 27% were measured at the -6 dB and -12 dB backoff levels [6]. Efficiencies at backoff points can be increased by optimizing the input drive conditions for the peaking amplifiers [7]. Moreover, further efficiency improvement of the three-stage Doherty amplifier at the maximum output power and backoff points can be achieved by using highly effective GaN HEMT devices and applying digital predistortion technique for linearization. In particular, the efficiency at the -12 dB output power backoff point was increased to more than 60% in this way [8].

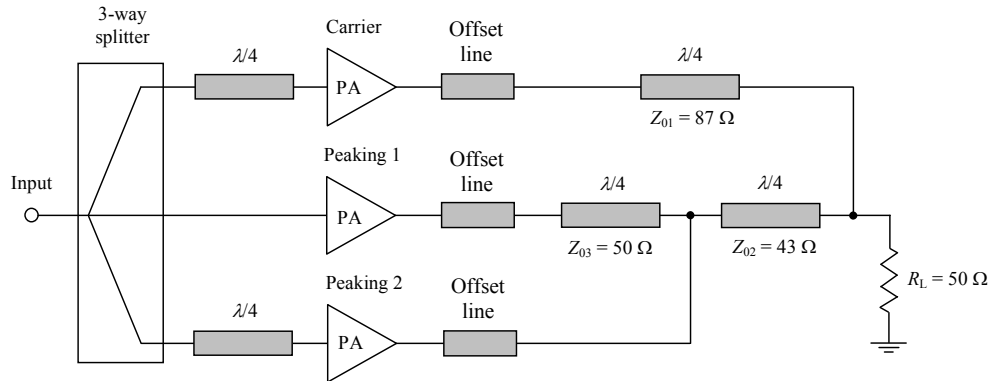


Fig. 3. Modified three-stage Doherty amplifier architecture.

A typical problem associated with the conventional three-stage Doherty amplifier is that the load-line modulation of the carrier stage stops at a certain power level, leaving the carrier amplifier in deep saturation and leading, consequently, to a significant degradation of its linear performance. In addition, when the carrier and peaking amplifiers have equal configurations with the same device periphery sizes, similar performance is obtained with regards to the symmetrical two-stage Doherty amplifier, with the efficiency peaking points at -3.5 dB and -6 dB backoff powers. These problems can be partially solved by using a modified three-stage Doherty amplifier architecture with a parallel combination of one carrier and one Doherty amplifier used as a peaking amplifier, as shown in Fig. 3 [9]. In this case, the novel way of combining enables a high instantaneous efficiency at -6 dB and -9.5 dB output backoff powers with a single device size. The characteristic impedances of the transforming quarterwave transmission lines are calculated as $Z_{01} = \sqrt{3} R_L$, $Z_{02} = (\sqrt{3}/2)R_L$, and $Z_{03} = R_L$, where R_L is the load resistance [10, 11].

Figure 4 shows the theoretical instantaneous drain efficiencies of the multistage (three and four stages) and four-way asymmetric Doherty power amplifier (DPA) architectures for different power (or device size) ratios, with peak efficiency ranging from -12 dB output power backoff levels. From Fig. 4 it follows that the multistage architecture provides significantly higher efficiency than the corresponding asymmetric one. Moreover, for a multistage Doherty configuration, lower efficiency peaking point can be achieved using an optimum device size ratio. For example, a peak efficiency at the lowest backoff of -12 dB is achieved for the device periphery ratio of 1:3:4 in a three-stage Doherty amplifier, while the lowest backoff of about -9.5 dB corresponds to the peak efficiency for equal device periphery size of 1:1:1 in a modified three-stage Doherty amplifier shown in Fig. 3 [6, 11].

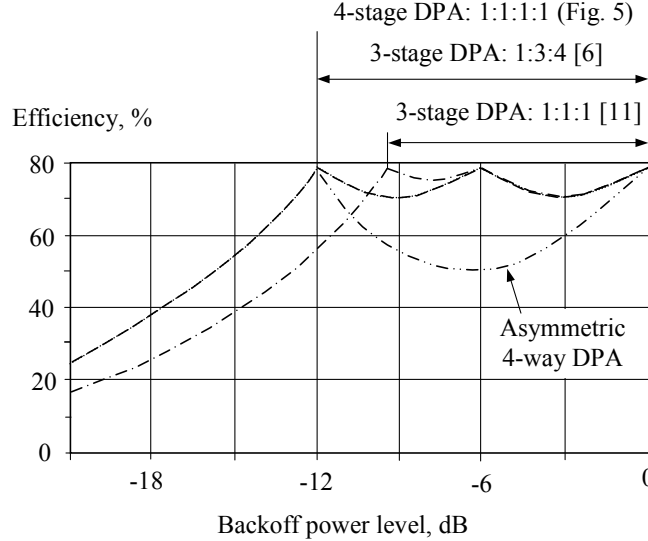


Fig. 4. Efficiencies of different Doherty amplifier architectures.

In a classical four-stage Doherty power amplifier with corresponding peak efficiencies at -6 dB, -12 dB, and -18 dB backoff levels, the maximum difference between characteristic impedances of the quarterwave transmission lines is equal to 16 [6]. For example, for load resistance $R_L = 6 \Omega$, the characteristic impedances of consecutive quarterwave transmission lines are equal to $Z_{01} = 12 \Omega$, $Z_{02} = 48 \Omega$, and $Z_{03} = 192 \Omega$, respectively, which is difficult to correctly fabricate as microstrip lines on a single substrate with fixed thickness and dielectric permittivity. In

a proposed four-stage Doherty configuration with the device size ratio of 1:1:1:1, where two conventional two-stage Doherty amplifiers are combined together in a final four-stage Doherty configuration (Doherty in Doherty), the maximum ratio between transmission-line characteristic impedances is equal to $(50 \Omega)/(25 \Omega) = 2$ only, as shown in Fig. 5. Figure 4 shows three theoretical efficiency peaking points provided by the modified four-stage Doherty amplifier with equal bias voltages for the first and second peaking amplifiers. However, their bias voltage optimization can change efficiency profile between 0-dB and -6 -dB backoff points and contribute to linearity improvement. This is a very practical version of a four-stage Doherty amplifier to achieve high output power with high drain efficiency using three 90° hybrid couplers at the input and four quarter-wavelength microstrip lines at the output.

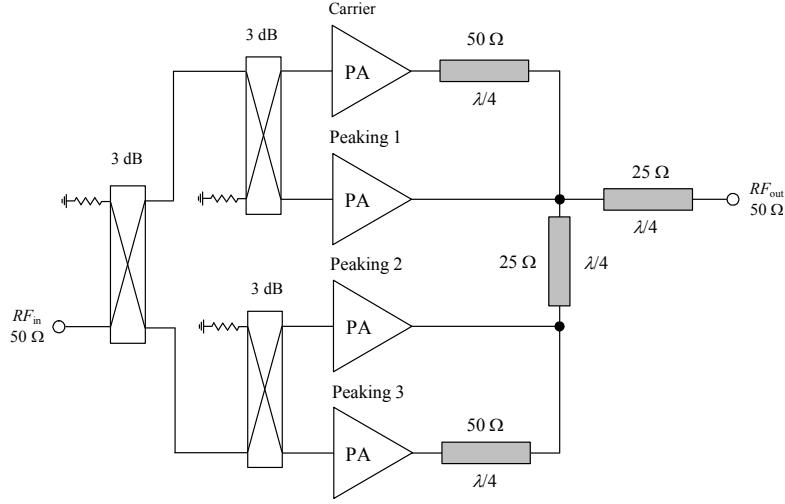


Fig. 5. A modified four-stage Doherty amplifier architecture.

Because of the device input and output parasitics such as the gate-source and drain-source capacitances, the outputs of the turned-off transistors in reality do not represent the open circuits, as well as the device input reactance varies with different bias voltage. Therefore, to compensate for these parasitic reactances, additional input offset lines can be implemented at the input of the peaking amplifiers and identical output offset lines which introduce the compensating inductive reactances can be connected in series to each output circuit [12].

INVERSE CLASS F

Figure 6(a) shows the transmission-line inverse Class-F load network, where the combined series transmission line $TL_1 + TL_2$ (together with an open-circuited capacitive stub TL_4 with electrical length of 30°) provides an impedance matching at the fundamental frequency between the equivalent optimum output device impedance R and load resistance R_L by proper choice of the transmission-line characteristic impedances Z_1 and Z_2 , where C_{out} and L_{out} are the elements of the matching circuit [13, 14].

The load network seen by the device multiharmonic current source at the second harmonic is shown in Fig. 6(b), where the shorting effect of the quarterwave short-circuited stub TL_3 is taken in to account. Here, the series transmission line TL_1 provides an open-circuit condition for the second harmonic at the device output by forming a second-harmonic tank together with C_{out} and L_{out} . Similar load network at the third harmonic is shown in Fig. 6(c), due to the open-circuit effect of the short-circuited quarterwave line TL_3 and short-circuit effect of the open-circuited har-

monic stub TL_4 at the third harmonic. In this case, the combined transmission line $TL_1 + TL_2$ (together with the series inductance L_{out}) provides a short-circuit condition for the third harmonic at the device output being shorted at its right-hand side. The electrical lengths of the transmission lines TL_1 and TL_2 can be defined from

$$2\omega_0 C_{out} - \frac{1}{2\omega_0 L_{out} + Z_1 \tan 2\theta_1} = 0 \quad (7)$$

$$3\omega_0 L_{out} + Z_1 \tan 3(\theta_1 + \theta_2) = 0 \quad (8)$$

with the maximum total electrical length $\theta_1 + \theta_2 = \pi/3$ or 60° at the fundamental frequency or 180° at the third harmonic component when $L_{out} = 0$.

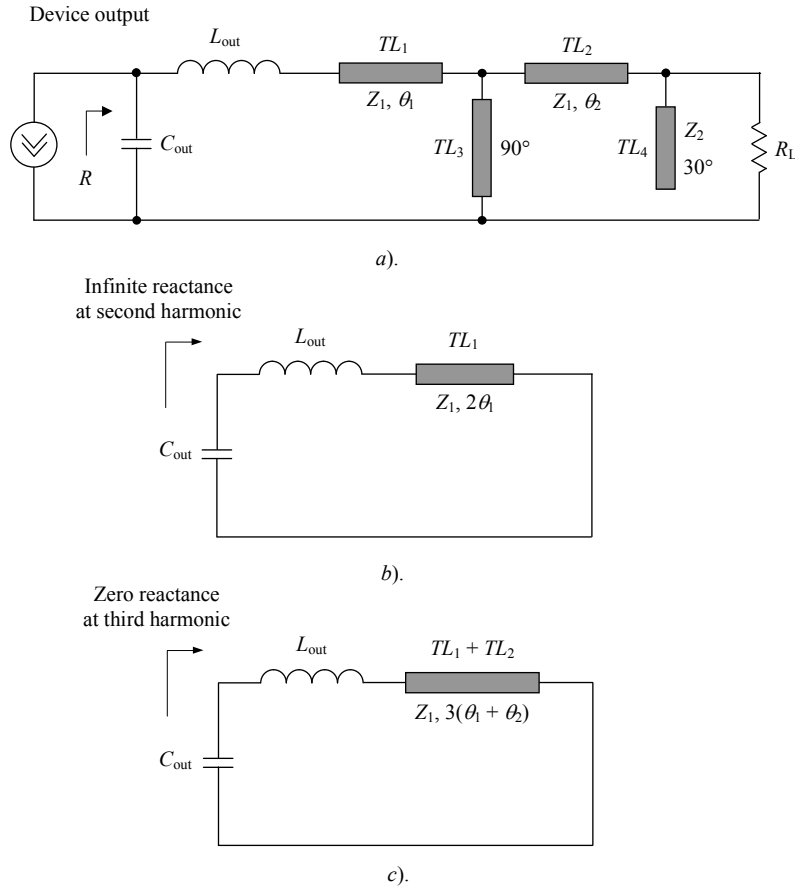


Fig. 6. Transmission-line inverse Class F load network.

Figure 7 shows the simulated circuit schematic of the transmission-line inverse Class F power amplifier based on a 25-W Cree GaN HEMT power transistor CGH40025F. The input matching circuit provides a complex-conjugate matching with the standard $50\text{-}\Omega$ source. The load network approximates the transmission-line structure with the second- and third-harmonic control shown in Fig. 6(a). In this case, the characteristic impedances of the shunt and series transmission lines were optimized for better performance and convenience of practical implementation. Special care was taken for modeling of the device input and output package leads to account for finite values of their inductances.

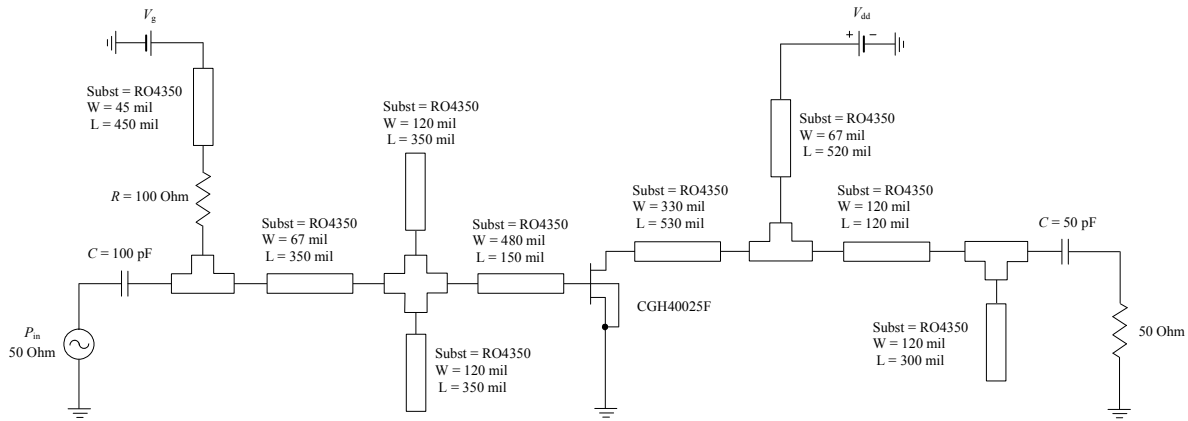


Fig. 7. Simulation setup of a 25-W inverse Class F GaN HEMT power amplifier.

Figure 8 shows the simulated results of an inverse Class F power amplifier using a 30-mil RO4350 substrate. The maximum output power of 43.4 dBm, drain efficiency of 84.6%, and PAE of 78.5% with a power gain of 11.4 dB (linear gain of about 17 dB) at $V_g = -2.5$ V and $V_{dd} = 28$ V were achieved at the operating frequency of 2.14 GHz.

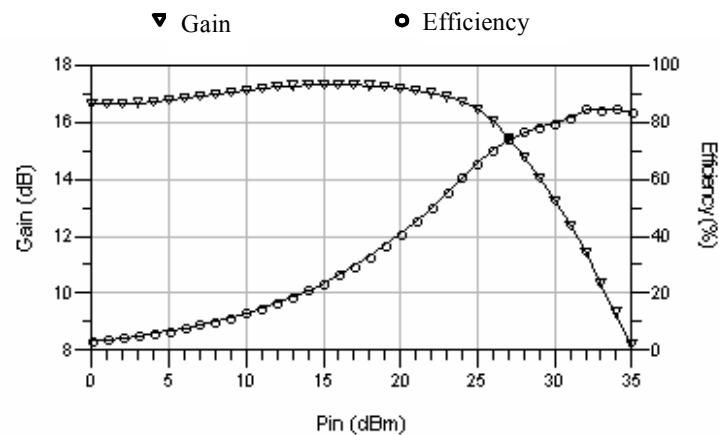


Fig. 8. Simulated power gain and drain efficiency.

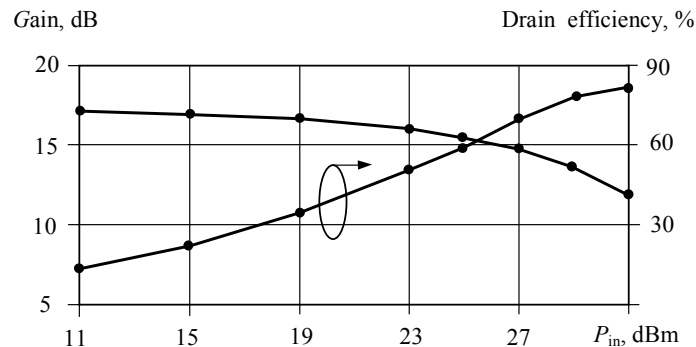


Fig. 9. Measured output power and drain efficiency versus input power.

Figure 9 shows the measured results of an inverse Class F GaN HEMT power amplifier fabricated on a 30-mil RO4350 substrate when a maximum output power of 43.5 dBm and a drain efficiency of 82.1% with a power gain of 12.2 dB at 2.14 GHz (quiescent current $I_q = 100$ mA

and drain supply voltage $V_{dd} = 32$ V) were achieved without any tuning of the input matching circuit and load network.

IMPLEMENTATION AND TEST

A novel high-efficiency 100-W four-stage Doherty structure based on 25-W inverse Class F power amplifiers was simulated and fabricated using a 30-mil RO4350 substrate. The simulated optimized drain efficiency and power gain versus output power for this architecture is shown in Fig. 10, from which it follows that high drain efficiency over 80% at saturation and more than 60% over 10-dB output power backoff levels are potentially achieved with optimum gate bias voltages for each transistor.

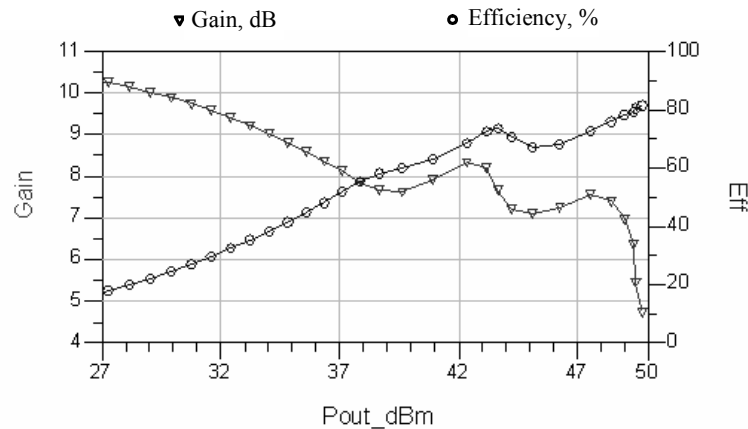


Fig. 10. Simulation results of a four-stage Doherty power amplifier.

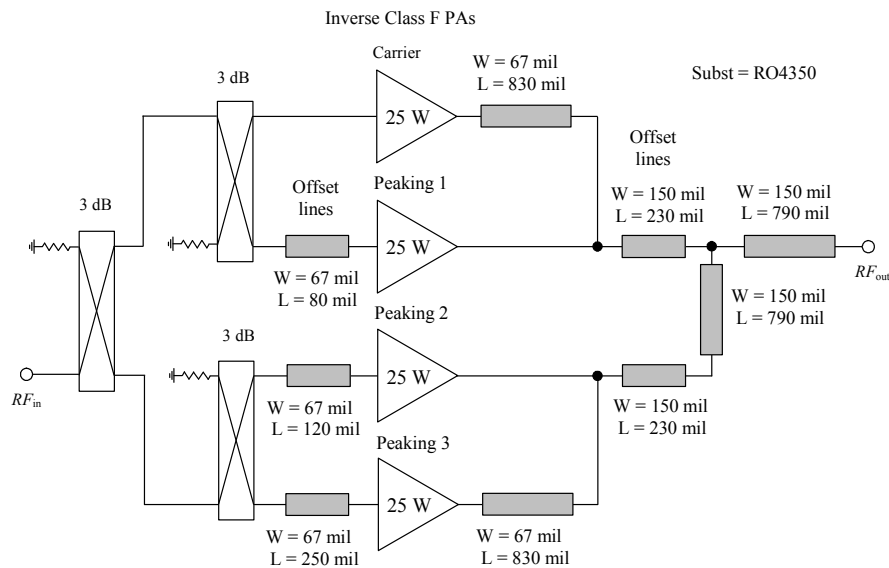


Fig. 11. Simplified practical topology of a 100-W four-stage Doherty GaN HEMT power amplifier.

Figure 11 shows the simplified practical topology of a novel 2.14-GHz four-stage Doherty power amplifier architecture based on four 25-W Cree GaN HEMT power transistors CGH40025F. The input dividing network includes three commercial 90° hybrid couplers. In a single-frequency CW operation mode when all transistors are biased with the same gate bias vol-

tage of -3.4 V, an output power of 50 dBm (100 W) and a drain efficiency of 77% were achieved at a dc supply voltage of 34 V.

In a single-carrier WCDMA operation mode with a PAR of 6.5 dB, a drain efficiency of 61% with a power gain of 6.7 dB was achieved at an average output power of 43 dBm (20 W), which corresponds to a 7-dB backoff from the saturated output power, as shown in Fig. 12. In this case, the adjacent channel leakage power ratio ($ACLR_1$) was measured at -31 dBc level, with the alternate channel leakage power ratio ($ACLR_2$) of -38.5 dBc, which is a promising starting point for applying a proper digital predistortion linearization technique.

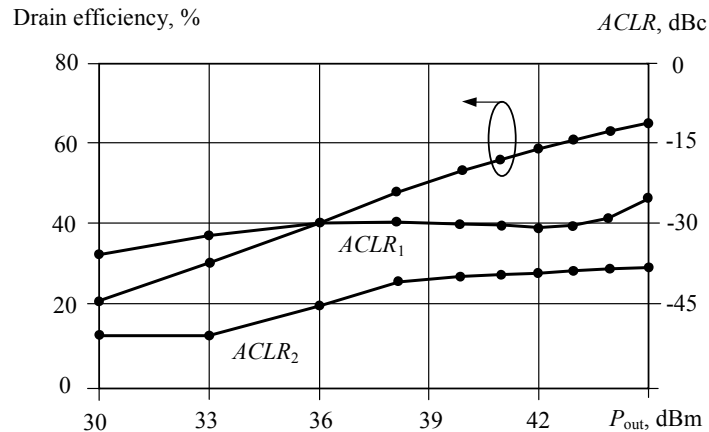


Fig. 12. Measured drain efficiency and $ACLR$ versus output power.

By optimizing the corresponding gate bias voltages ($V_g = -2.85$ V, $V_{g1} = V_{g2} = -6.6$ V, and $V_{g3} = -4.3$ V) and resistances in the gate bias circuits of the carrier and three peaking amplifiers, a power gain can be increased up to 8.0 dB with a drain efficiency of 58.5% and a PAE of 49% when the $ACLR_1$ of -32 dBc and $ACLR_2$ of -42 dBc can be achieved.

CONCLUSION

The novel high-efficiency four-stage Doherty power amplifier architecture for base station applications for modern communication standards such as CDMA2000, WCDMA, or OFDM has been proposed and fabricated. In practical verification, each power amplifier is based on a 25-W Cree GaN HEMT device with the transmission-line load network corresponding to an inverse Class F mode approximation. In a CW operation mode with the same bias voltage for each transistor, an output power of 50 dBm with a drain efficiency of 77% was achieved at a supply voltage of 34 V. In a single-carrier WCDMA operation mode with PAR of 6.5 dB, a high drain efficiency of 61% was achieved at an average output power of 43 dBm, with $ACLR_1$ measured at -31 dBc level.

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