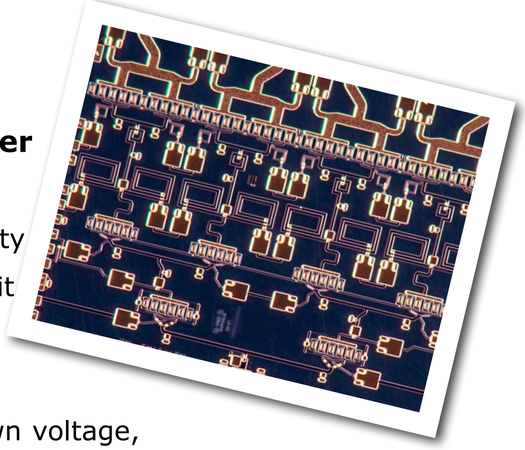
PRELIMINARY

CMPA1D1E030D

30 W, 13.75 - 14.5 GHz, 40 V, GaN MMIC, Power Amplifier



Cree's CMPA1D1E030D is a gallium nitride (GaN) High Electron Mobility Transistor (HEMT) based monolithic microwave integrated circuit (MMIC) on a silicon carbide substrate, using a 0.25 μm gate length fabrication process. GaN-on-SiC has superior properties compared to silicon, gallium arsenide or GaN-on-Si, including higher breakdown voltage, higher saturated electron drift velocity and higher thermal conductivity. GaN HEMTs also offer greater power density and wider bandwidths compared to Si, GaAs, and GaN-on-Si transistors.

Typical Performance Over 13.75-14.5 GHz (T_C = 25˚C)

Parameter	13.75 GHz	14.0 GHz	14.5 GHz	Units
Small Signal Gain	27	26	25	dB
P_{SAT} @ P_{IN} = 26 dBm	33	34	30	W
P_{3dB} Backoff @ P_{IN} = 20 dBm	20	20	16	W
PAE @ P_{IN} = 26 dBm	24	23	22	%
PAE @ P_{IN} = 20 dBm	22	21	20	%

Note: All data in this table is based on fixtured, CW performance.

Features

- 27 dB Small Signal Gain
- 30 W Typical P_{SAT}
- Operation up to 40 V
- High Breakdown Voltage
- High Temperature Operation

Applications

- Satellite Communications Uplink

Rev 0.0 – April 2015

Absolute Maximum Ratings (not simultaneous) at 25˚C

Parameter	Symbol	Rating	Units	Conditions
Drain-source Voltage	V_{DSS}	84	V_{DC}	25˚C
Gate-source Voltage	V_{GS}	-10, +2	V_{DC}	25˚C
Storage Temperature	T_{STG}	-55, +150	˚C	
Operating Junction Temperature	T_J	225	˚C	
Maximum Forward Gate Current	I_{GMAX}	10	mA	25˚C
Maximum Drain Current[1]	I_{DMAX}	0.6	A	Stage 1, 25˚C
Maximum Drain Current[1]	I_{DMAX}	0.96	A	Stage 2, 25˚C
Maximum Drain Current[1]	I_{DMAX}	2.2	A	Stage 3, 25˚C
Thermal Resistance, Junction to Case[2]	$R_{\theta JC}$	1.5	˚C/W	85˚C, P_{DISS} = 94W
Mounting Temperature (30 seconds)	T_S	320	˚C	30 seconds

Note[1] Current limit for long term, reliable operation. Total current when biased from top and bottom drain pads.
Note[2] Eutectic die attach using 80/20 AuSn mounted to a 20 mil thick CuMoCu carrier.

Electrical Characteristics (Frequency = 13.75 GHz to 14.5 GHz unless otherwise stated; T_C = 25˚C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics						
Gate Threshold	V_{TH}	-3.8	-2.8	-2.3	V	V_{DS} = 10 V, I_D = 18.2 mA
Drain-Source Breakdown Voltage	V_{BD}	84	100	–	V	V_{GS} = -8 V, I_D = 18.2 mA
RF Characteristics[2]						
Small Signal Gain	S21	–	27	–	dB	V_{DD} = 40 V, I_{DQ} = 300 mA
Input Return Loss	S11	–	-16	–	dB	V_{DD} = 40 V, I_{DQ} = 300 mA
Output Return Loss	S22	–	-9	–	dB	V_{DD} = 40 V, I_{DQ} = 300 mA
Power Output	P_{OUT1}	–	50	–	W	V_{DD} = 40 V, I_{DQ} = 300 mA, CW, P_{IN} = 24 dBm
Power Output	P_{OUT2}	–	24	–	W	V_{DD} = 40 V, I_{DQ} = 300 mA, P_{IN} = 18 dBm
Power Added Efficiency	PAE_1	–	30	–	%	V_{DD} = 40 V, I_{DQ} = 300 mA, CW, P_{IN} = 24 dBm
Power Added Efficiency	PAE_2	–	25	–	%	V_{DD} = 40 V, I_{DQ} = 300 mA, P_{IN} = 18 dBm
Power Gain	G_P	–	22	–	dB	V_{DD} = 40 V, I_{DQ} = 300 mA
Output Mismatch Stress	VSWR	–	5 : 1	–	Ψ	No damage at all phase angles, V_{DD} = 40 V, I_{DQ} = 300 mA, P_{OUT} = 25W CW

Notes:
[1] Scaled from PCM data.
[2] All data pulse tested on-wafer with Pulse Width = 10 μs, Duty Cycle = 0.1%.

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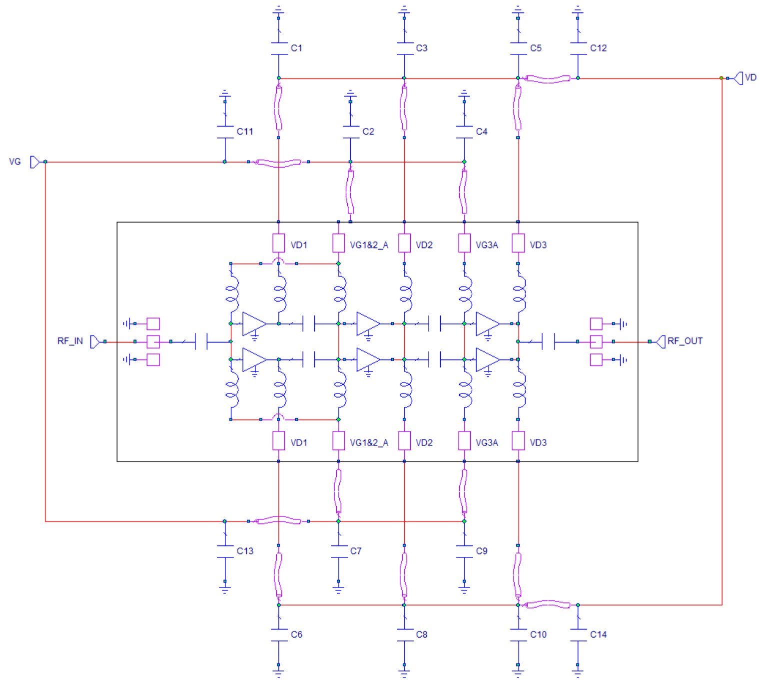
Block Diagram Showing Additional Capacitors for Operation Over 13.75 to 14.5 GHz



Designator	Description	Quantity
C1,C2,C3,C4,C5,C6,C7,C8,C9,C10	CAP, 51pF, +/-10%, SINGLE LAYER, 0.030", Er 3300, 100V, Ni/Au TERMINATION	10
C11,C12,C13,C14	CAP, 680pF, +/-10%, SINGLE LAYER, 0.070", Er 3300, 100V, Ni/Au TERMINATION	4

Notes:

[1] The input, output and decoupling capacitors should be attached as close as possible to the die- typical distance is 5 to 10 mils with a maximum of 15 mils.

[2] The MMIC die and capacitors should be connected with 2 mil gold bond wires.

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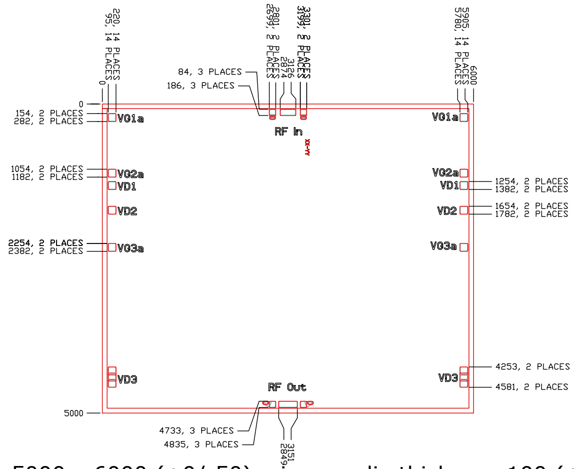
Die Dimensions (units in microns)



Overall die size 5000 x 6000 (+0/-50) microns, die thickness 100 (+/-10) microns.
All Gate and Drain pads must be wire bonded for electrical connection.

Pad Number	Function	Description	Pad Size (in)	Note
1	RF_IN	RF-Input pad. Matched to 50 ohm	102x252	5
2	VG1A bottom	Gate control for stage1. Vg = -2.0 to -3.5 V	128x125	1,2
3	VG1A top	Gate control for stage1. Vg = -2.0 to -3.5 V	128x125	1,2
4	VG2A bottom	Gate control for stage2. Vg = -2.0 to -3.5 V	128x125	1,2
5	VG2A top	Gate control for stage2. Vg = -2.0 to -3.5 V	128x125	1,2
6	VD1 bottom	Drain control for stage1. Vd = 40 V	128x125	1,3
7	VD1 top	Drain control for stage1. Vd = 40 V	128x125	1,3
8	VD2 bottom	Drain control for stage2. Vd = 40 V	128x125	1,4
9	VD2 top	Drain control for stage2. Vd = 40 V	128x125	1,4
10	VG3A bottom	Gate control for stage3. Vg = -2.0 to -3.5 V	128x125	1,2
11	VG3A top	Gate control for stage3. Vg = -2.0 to -3.5 V	128x125	1,2
12	VD3 bottom	Drain control for stage3. Vd = 40 V	328x125	1,4
13	VD3 top	Drain control for stage3. Vd = 40 V	328x125	1,4
14	RF_OUT	RF-Output pad. Matched to 50 ohm	102x302	5

Notes:

[1] Attach bypass capacitor to pads 2-13 per aplications circuit

[2] VG1A&2A&3A top and bottom are connected internally, so it would be enough to connect either one for proper operation

[3] VD1 top and bottom are not connected internally and have to be biased from both sides for proper operation

[4] For current handling, it is recommended to bias VD2 and VD3 from both top and bottom sides

[5] The RF Input and Output pads have a ground-signal-ground with a nominal pitch of 10 mil (250 um). The RF ground pads are 102 x 102 microns

Die Assembly Notes:

- Recommended solder is AuSn (80/20) solder. Refer to Cree's website for the Eutectic Die Bond Procedure application note at http://www.cree.com/~/media/Files/Cree/RF/Application%20Notes/Appnote%202%20Eutectic.pdf
- Vacuum collet is the preferred method of pick-up.
- The backside of the die is the Source (ground) contact.
- Die back side gold plating is 5 microns thick minimum.
- Thermosonic ball or wedge bonding are the preferred connection methods.
- Gold wire must be used for connections.
- Use the die label (XX-YY) for correct orientation.

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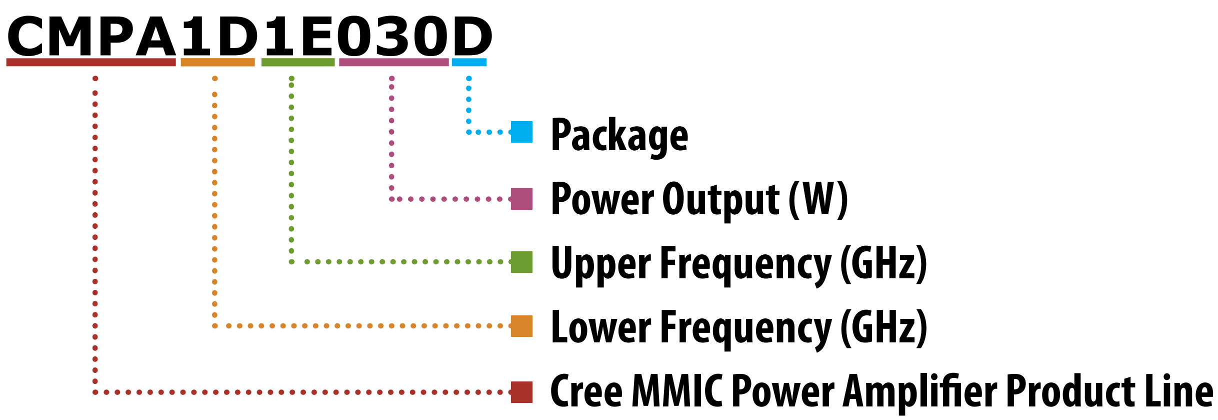
Part Number System



Parameter	Value	Units
Lower Frequency	13.75	GHz
Upper Frequency[1]	14.5	GHz
Power Output	30	W
Package	Bare Die	-

Table 1.

Note[1]: Alpha characters used in frequency code indicate a value greater than 9.9 GHz. See Table 2 for value.

Character Code	Code Value
A	0
B	1
C	2
D	3
E	4
F	5
G	6
H	7
J	8
K	9
Examples:	1A = 10.0 GHz 2H = 27.0 GHz

Table 2.

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