A Comparison between Class E Power Amplifiers employing LDMOS FETs and SiC MESFETs

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Abstract

This paper demonstrates the use of optimized analytical procedures to design lossy Class E amplifiers at 1 and 2 GHz using Si LDMOS FETs and SiC MESFETs respectively. The designs use new large-signal models for the LDMOS FETs and SiC MESFETs which provide accurate simulations in both deep sub-threshold (Class C) and fully RF driven "on" states. Drain efficiencies of 67% are achieved for an LDMOS FET Class E, 9 watt amplifier with 15.7 dB gain at 1 GHz with a corresponding 60% drain efficiency at 11 watts of output power and 14.25 dB gain at 2.14 GHz using a commercially available SiC MESFET. The paper will review the properties of wide bandgap transistors that need to be addressed to optimize their performance in Class E and Class S amplifier and modulator applications.

Introduction

The Class E amplifier is a switch-mode amplifier which can provide very high drain efficiency because the drain voltage is minimized when the drain current is high [1]. Class E amplifiers have been designed up to about 5 GHz using transistor technologies such as MESFET and HBT. These amplifiers are limited to low powers because the technologies have low breakdown voltages and low power densities. Recently, Class E amplification has been demonstrated with 10 watt LDMOS FETs at 1 GHz with drain efficiencies of almost 70% [2].

Analysis

Figure 1 shows an ideal Class E amplifier circuit where it is assumed that switch off-resistance is high i.e. there is no current through the switch during the off-state and that the switching-on resistance R_S is constant, the output capacitance C_{DS} is independent of the switch voltage and the Q factor of the output circuit is large enough to suppress the harmonics.

R_L and L2 of Figure 1 can be evaluated for a particular switching frequency from [3]

$$P_{OUT} = (I_O^2/2)R_L \text{ and } L2 = Q_L R_L/\omega_C$$

Assuming P_{OUT} = 8 watts and I_O is 1.5 amps results in R_L being 8 ohms. Assuming Q_L = 5, in order that the circuit has low sensitivity to the series resonator values, results in L2 being 1.5 nH for operation at 2 GHz.

Further, C2 can be evaluated using the expression C2 ~ $1/(\omega_C^2 L2)$ [3] leading to a value of 4 pF. These component values can be used as starting points in

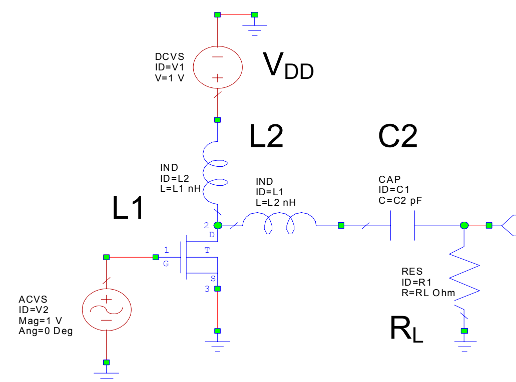

Fig. 1. Ideal Class E Amplifier

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simulations using accurate large signal models for the transistors. An approximation to the expected efficiency of the amplifier can be provided by using the expression of Alinikula [4] whereby $R_{ON} < 0.1V_{DD}^2/P_{OUT}$. In the cases of LDMOSFETs and SiC MESFETs with drain voltages of 26 and 48 volts, the on-resistances must be less than 6.7 ohms and 23 ohms respectively. In both these cases the drain efficiency would be 54%. Clearly the R_{ON} of the transistors needs to be as low as possible to maximize drain efficiency – the actual effective R_{ON}'s are available as a result of complete large-signal simulations.

Results

Two Class E amplifiers have been designed at 1 GHz and 2.14 GHz using commercially available packaged power transistors from Cree Microwave – the UGF2010 Si LDMOS FET and the CRF24010 SiC MESFET respectively. The actual Class E circuits exemplified in this paper are slightly different when compared to the ideal case of Figure 1. The circuit topology is adjusted to ensure that the output capacitance of the transistor is completely absorbed and that the RF load which is about 8 ohms is transformed to 50 ohms by a 2-stage transformation network. The input match of the amplifier was implemented using a series inductor and parallel capacitor in the case of the LDMOS FET circuit and an ideal source pull tuner for the SiC MESFET case. The complete amplifier circuits for the two cases can be seen in Figures 2 and 3.

Two new large signal models have been used in the following simulations – the so-called Cree/Modelithics/Curtice [5] model for the LDMOS FET which features a continuous 4 region model covering sub-threshold, quadratic, linear

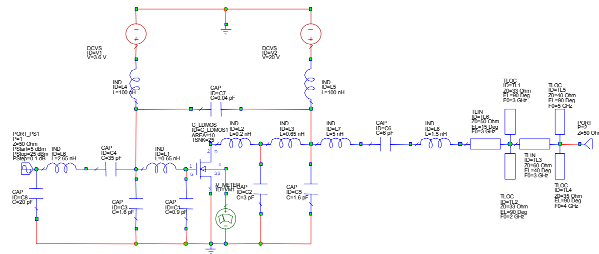

Fig. 2. LDMOS FET Class E Amplifier

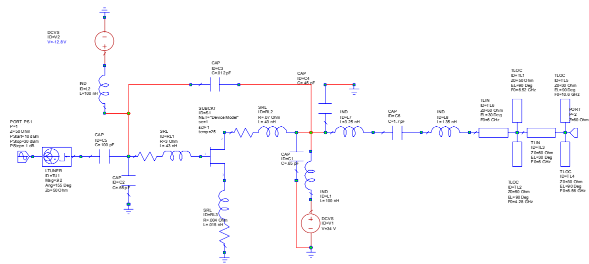

Fig. 3. SiC MESFET Class E Amplifier

and compression operation and efficient capacitance versus voltage expressions [6, 7]. This model implementation results in a wideband capability necessary to accurately predict harmonic content; is scaleable up to at least a 30:1 ratio in transistor size; predicts IMDs well with high dynamic range including predicting correct parameters even in Class B and C; includes dynamic self heating and uses efficient coding and extraction. The SiC MESFET model uses a modified Curtice Cubic approach and has been developed internally at Cree [8].

All the simulations were performed using Microwave Office from AWR. The load networks were optimized for highest PAE and output power. Figure 4 shows the simulated output power and PAE versus input power for the LDMOS FET Class E amplifier. The circuit

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topology gives a maximum drain efficiency of 69% at an output power of 8.7 watts with 15.7 dB gain at 1 GHz.

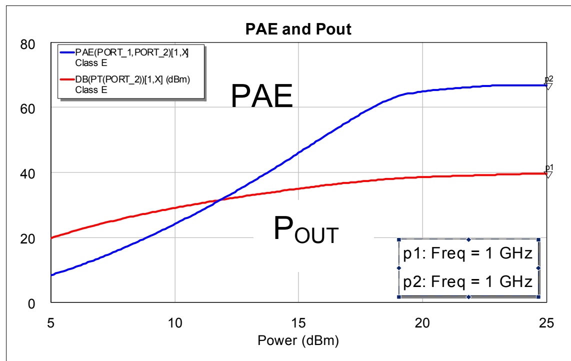

Fig. 4. PAE and Output Power vs. Input Power for LDMOS FET Class E Amplifier

V_{DD}	PAE, %	Output Power, Watts
8	62	1.67
10	65.6	2.56
12	67	3.57
14	67.2	4.67
16	67.2	5.85
18	67	7.13
20	66.8	8.51
22	66.1	10
24	65	11.4
26	63.6	12.6
28	62	14.2

Fig. 5. PAE and Output Power vs. DC Supply Voltage for LDMOSFET Amplifier

Figure 5 shows the PAE and P_{OUT} of the amplifier as a function of V_{DD}. The maximum drain voltage recommended for the LDMOS FET is 28 volts. Calculation of R_{ON} results in an effective value of 4 ohms for the transistor.

Figure 6 shows the simulated power and PAE versus input power for the SiC MESFET Class E amplifier. The circuit topology gives a maximum drain efficiency of 62% at an output power of 11 watts with 14.25 dB gain at 2.14 GHz.

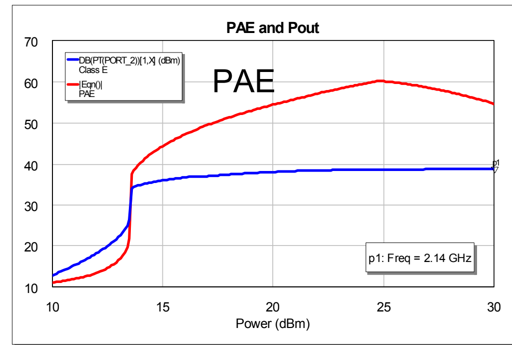

Fig. 6. PAE and Output Power vs. Input Power for SiC MESFET Amplifier

Figure 7 shows the PAE and P_{OUT} of the amplifier as a function of V_{DD}. The maximum recommended drain voltage for the SiC MESFET is 48 volts.

V_{DD}	PAE, %	Output Power, Watts
20	44	1.9
22	47.4	2.4
24	50.5	3
26	52.8	3.7
28	54.7	4.44
30	56.4	5.24
32	58	6.1
34	59	7
36	60	7.94
38	60.6	8.8
40	60.7	9.7
42	61	10.7
44	61.2	11.75
46	61.5	12.9
48	61.2	13.9

Fig. 7. PAE and Output Power vs. DC Supply Voltage for SiC MESFET Amplifier

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Calculation of R_{ON} results in an effective value of 14.7 ohms for the transistor. This relatively high value for R_{ON} results from the high knee/threshold voltages for SiC MESFETs as well as the present transistor technology being optimized for Class A/B and Class A amplifier applications. However, the simulated performance of this Class E amplifier at 2 GHz shows great promise for the employment of both SiC and GaN based technologies in Class E and Class S amplifiers and modulators.

Conclusions

Comparisons between LDMOS FET and SiC MESFET based Class E amplifiers have been made. It has been shown that SiC MESFET Class E amplifiers show promise for operation in high efficiency power amplifiers in 3G bands. A Class E amplifier at 2.14 GHz, employing a commercially available SiC MESFET transistor, has been compared directly with an LDMOS FET amplifier at 1 GHz indicating that drain efficiencies of 60% should be possible. With further reduction in transistor on-resistance, efficiencies of well over 70% should be possible with the promise of such wide bandgap transistors being employed in 4G systems at frequencies in the 3.5 GHz range.

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