Commercial GaN Devices For Switching and Low Noise Applications

Raymond Pengelly, Scott Sheppard, Thomas Smith, Bill Pribble, Simon Wood and Carl Platis

Cree Inc. Research Triangle Park, NC 27709 USA email: ray_pengelly@cree.com

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Abstract

Gallium nitride (GaN) RF power transistor and MMIC technologies have become sufficiently mature and reliable in the last few years that there are now large numbers of fielded devices in both military and commercial applications. Wide bandgap technology is now finding extended use in switching, control and low noise applications. Cree's GaN on silicon carbide (SiC) MMIC processes provide high drain to source breakdown voltage (typically 150 volts) resulting in robust transistor operation allowing, for example, simpler receiver protection circuitry. In addition high output impedances enable large bandwidth of operation; high output third order intercept (TOI) enables lower distortion and higher dynamic range receivers; low noise figures similar to GaAs MESFETs coupled with high f_T (25 GHz) enable multi-stage LNA's to be produced. Application areas for GaN switches, control components and low noise amplifiers include electronically scanned arrays, both military and commercial communications as well as jammers.

INTRODUCTION

The two traditional technologies currently used for RF switching are based on either PiN diodes or GaAs FETs. The FET has the advantage of low insertion loss and high switching speed performance with a minimal DC-bias power requirement needed for the switching action. In contrast the PiN diode with its vertical structure has the advantage of higher power handling capability. A key limitation of GaAs technology used for FET switches is the relatively low electric field strength of this material. For the short Source-Drain separation that high frequency performance demands this implies a low breakdown voltage and in turn a limited power handling capability, typically in the range of a few watts. The advent of new device technology based on GaN material, for which a key property is high electric field strength, promises to significantly enhance the power handling capability of FET based switches [1, 2]. A key advantage of the FET is its ease of integration in standard MMIC architectures - as such GaN provides the enabling technology for advanced, high power control in fully integrated RF circuits.

The overall noise figure for a system is typically dominated by the input stage so it is, therefore, critical that the amplifier close to the detection system is low noise and high gain. In addition it must be robust enough to handle the dynamic range of the signals that can occur at the input. Again the properties of GaN make it an ideal material for such applications. GaN HEMTS have been shown to have similar noise figures to their GaAs counterparts; the high electric field strength makes them extremely robust with high dynamic range, while the high impedance allows for broadband capability. The combination of high power RF switching together with extremely robust low noise amplifiers provides an enabling technology for the development of highly integrated Tx/Rx units.

Cree Inc. has been a pioneer in the development of high performance microwave devices based on GaN and have expanded the portfolio of available devices to include a broad range of power levels as well as advanced MMICs with very wide bandwidth capability [3]. With the increasing maturity of the available technology GaN is now being applied to low noise amplifiers and RF power control [4].

This paper describes the use of Cree's non-linear power switch model enabling the accurate design of a variety of multi-pole, multi-throw switches. A number of MMIC switch examples are provided including a commercially available DC to 3 GHz, 25 watt single-pole (CMSA30025S), double throw switch. Additionally, the recently developed noise modeling capability allows for the design of advanced LNA MMICs and results are presented showing good agreement between measured and modeled noise parameters for both 0.4 and 0.25 micron gate length HEMTs.

GaN FET SWITCH APPROACH

The use of a FET as a switch results from the fact that the path between Source and Drain can be seen as a voltage controlled resistance. In contrast to the situation when the FET is used as an amplifier there is no DC bias applied to source or drain. A DC bias applied to the gate controls the "opening and closing" of the switch. As the ability to control the current through the switch should be independent of the current flowing, then it can be seen that a large gate resistance is necessary for isolation between the control and RF signals. In addition to the variable resistance there is also a capacitance associated with the FET which is dependent on the size of the device, but also on the process used for manufacture. The value of this capacitance determines the high frequency isolation achieved; a small device will have improved high frequency capability, but also increased insertion loss in the on-state. In its simplest form the switch model can therefore be represented by a simple variable resistor and capacitor in the path of the RF signal - in practice a more complex model that takes account of the parasitics associated with each terminal (resistive, capacitive and inductive) is used. Figure 1 illustrates the equivalent circuit model used in the design of RF switches. Lumped element parameters have been extracted using on-wafer s-parameter measurements; a scaled polynomial is then fitted to the extracted capacitance and resistance values.

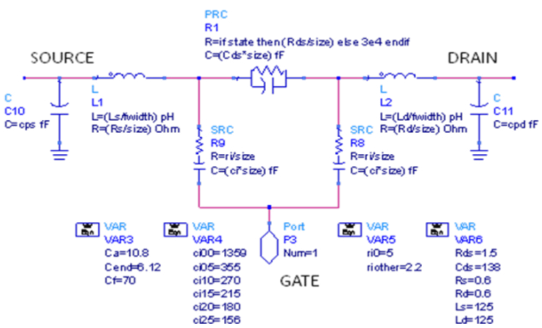

Figure 1. Schematic of the equivalent circuit used for a FET RF switch.

Bias dependent gate capacitance is measured using CV measurements. In the off-state the series capacitance of the gate to source (Cgs) and drain to gate (Cdg) form an RF potential divider. Assuming that the two capacitance values are equivalent the potential is equally divided (Vgs=Vdg). The potential at the gate relative to either source or drain is equal to the sum of the DC applied bias Vgg and the corresponding RF potential. The switch remains in a strongly isolating state provided that the summed potential does not exceed the breakdown voltage of the junction during the negative swing of the RF signal or exceed the pinch-off potential in the positive swing. At low frequencies the reactance of Cgs (or Cgd) can become large as compared to the gate resistance, as a result the gate resistance effectively shorts out one of the capacitances with the result that the high power isolation is compromised. The lower the gate resistance the higher the frequency at which this happens. Low frequency operation is thus limited by gate leakage. For a MESFET or HEMT technology in which the gate contact is not isolated from the channel the lower frequency cut-off is typically > 100MHz and this limitation also applies to GaN technology.

Figure 2 shows the design and layout of the Cree CMSA30025 switch MMIC - the layout is a relatively standard single Series/ Shunt SPDT design and includes via-holes to minimize the impedance to ground for the shunt FET. The performance of the switch (Figure 3), which is the first in a series of GaN control devices to be commercially released, is capable of handling 25 Watts at its 0.1 db compression point and has less than 0.7 dB insertion loss with a typical isolation of better than 30 dB and TOI of 60 dBm. When packaged in a low cost plastic QFN surface mount package it has a typical "hot" switching speed of less than 20 nanoseconds. The device is based on the manufacturing technology that has been reliably demonstrated for GaN transistors used in power amplifier applications - for switching applications, however, the transistor layout is different. For a transistor used for amplification the gate is placed close to the source contact, whereas in the case of a switching device the gate is symmetrically placed between source and drain. Present switch products use a standard Schottky diode gate structure and RF power handling at low frequencies is limited by the gate leakage. This can be clearly seen in the signal compression characteristics of Figure 3.

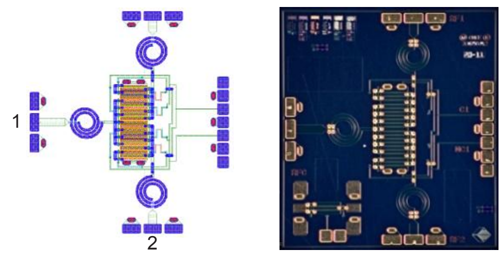

Figure 2. Design and implementation of the CMSA30025 SPDT MMIC switch.

The same core technology has been extended to other MMIC switch designs including a 20 watt, DC to 3 GHz SP4T and a 2 MHz to 2500 MHz SPDT/DP5T - see Figures 4 and 5 respectively. All of these designs demonstrate the combination of high power handling enabled by the use of GaN together with the advantages of FET design namely low DC power consumption, small size and need for few external components compared to PIN diodes. Successful demonstrations of

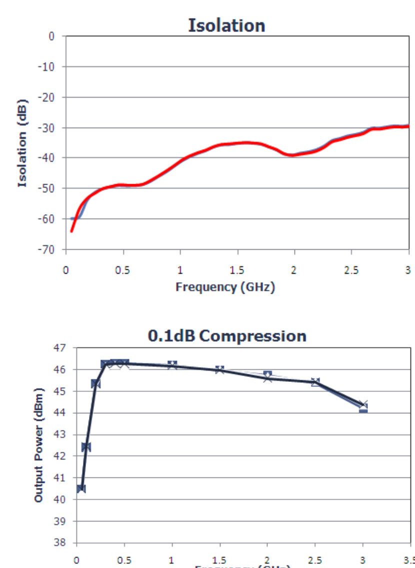

Figure 3. Performance of commercially available CMSA30035S GaN MMIC switch.

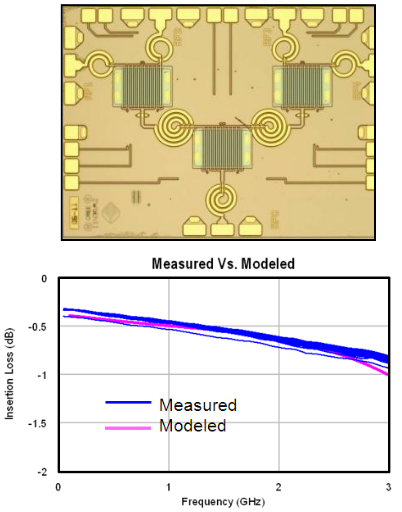

Figure 4. SP4T GaN 20W Switch MMIC. Excellent agreement is achieved with Cree's non-linear switch model.

2nd generation switches that utilize an insulated gate (MISHFET) structure, which significantly reduces gate leakage and extends the lower frequency limit for operation, have also been shown.

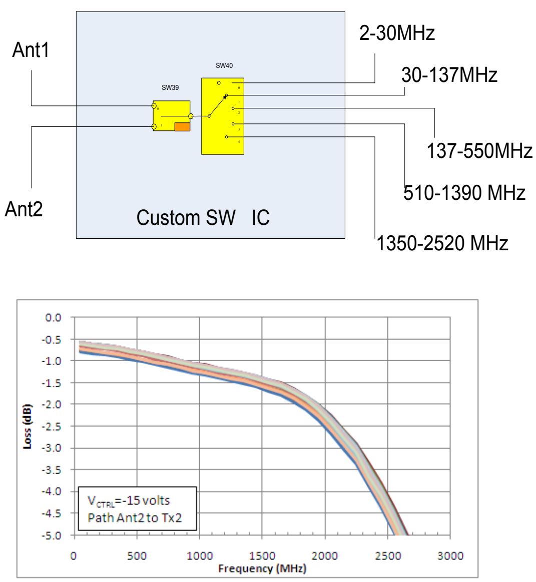

Figure 5. DP5T GaN Switch MMIC. Demonstrates functionality of GaN MMIC approach, small size (3.57 x 3 mm).

LOW NOISE AMPLIFIERS IN GaN

The typical criteria in selection of a transistor for a Low Noise Amplifier (LNA) design are high gain, low minimum noise figure and high 3rd order intercept (TOI) - GaN HEMTs fulfill all these criteria and appear as ideal candidates for such applications. To date GaN transistors have created the most attention in their suitability for high power applications, which perhaps explains the relatively smaller volume of work on lower power LNA's. Studies to date have shown that the typical noise figure achieved for a GaN HEMT can be compared to an equivalent GaAs transistor. The key motivations for using GaN technology are the extreme robustness of the device, opening the path

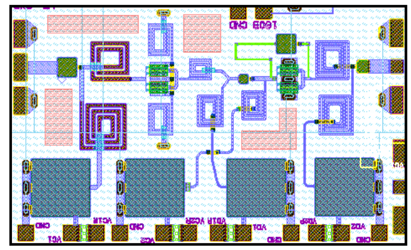

Figure 6. Design of 2/stage LNA MMIC. Compact design achieved 1.7 x 2.7mm size.

for receiver circuits where the need for (lossy) limiters can be either reduced or completely excluded, and the ability to integrate the functionality into high power MMIC designs [5, 6, 7 and 8]. One of the first commercially available GaN LNA MMICs (CMLA2540001) was recently released by Cree. (see Figure 6). The LNA MMIC is a 2-stage S-Band design that demonstrates a noise figure over the 2.5 to 4.5 GHz band of less than 2 dB with 30 dB gain and an output TOI of greater than 38 dBm when operating at V_{DS} = 24V. The circuit has been designed using the available transistor models and excellent agreement between modeled and measured performance has been achieved (see Figure 7).

T/R MODULE PHASE AND GAIN CONTROL COMPONENTS

Besides HPA's, LNA's and switches, attenuators and phase shifters have also been realized as GaN HEMT based MMICs. Table 1 shows a summary of some of the performances achieved with S-Band GaN MMIC components that have been designed and manufactured by Cree.

Component	6 Bit Attenuator	6 Bit Phase Shifter	LNA	Power Amplifier	T/R Switch
Frequency (GHz)	2.7 to 3.5	2.7 to 3.5	2.7 to 3.5	3.0 to 3.5	2.7 to 3.5
Pout or TOI	51dBm	51dBm	34.5dBm OTOI	40 watts	>20 watts
Gain/Loss	-4.9dB	-5.6dB	25dB	25dB	-.75dB
NF or PAE			1.2dB NF	60% PAE	
Size (mm)	2.5x3	3x3	3.2x2.3	4.2x3	2x2

Table 1. Summary of Performances of S-Band GaN MMIC Control Components

CONCLUSIONS

GaN has established itself as a mainstream semiconductor technology for the manufacture of RF devices for power amplifiers - this capability is now being extended with the commercial release of both high

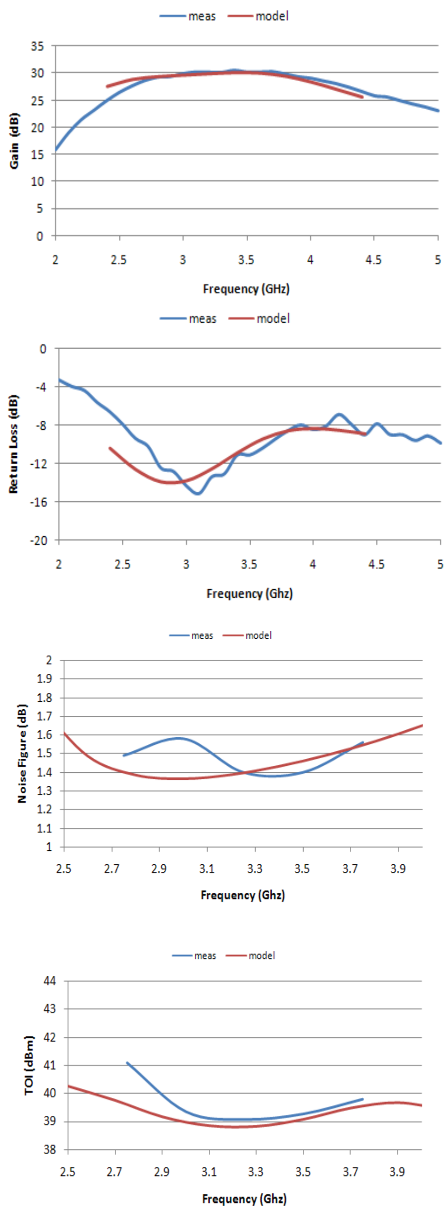

Figure 7. Performance of the LNA MMIC shown in Figure 6. Good agreement is achieved with the simulation results.

power switches for RF control and low noise amplifiers. As with power amplifiers the GaN material enables a substantial extension in performance compared with traditional technologies. A number of examples have been discussed that illustrate the performance of a number of different switch configurations and the good agreement achieved between modeled and measured parameters. The availability of the various building blocks for RF systems on chip (SoC) in GaN technology has opened the path to complex MMIC designs - the integration of LNA, switch and PA into single MMICs for advanced Rx/Tx units will be a key production driver in the next few years [9 and 10].

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ACRONYMS

HEMT: High Electron Mobility Transistor
SPDT: Single Pole, Double Throw
SP4T: Single Pole, Four Throw
DP5T: Double Pole, Five Throw
OTOI : Output Third Order Intercept
LNA: Low Noise Amplifier
PA: Power Amplifier
MISHFET:Metal–Insulator–Semiconductor Heterostructure Field-Effect Transistor
T/R: Transmit/Receive