Design of a High Power Doherty Amplifier Using a New Large Signal LDMOS FET Model

Simon M. Wood
Cree Microwave Inc.
simon_wood@cree.com

Raymond S. Pengelly
Cree Microwave Inc.
ray_pengelly@cree.com

Abstract

There have been a number of papers written recently on the use of the Doherty amplifier technique at microwave frequencies. These have been for the purposes of increasing efficiencies in high peak to average ratio applications such as W-CDMA. Many of these papers have dealt with relatively low power levels where classical Doherty design formulae can be applied. This paper describes the use of a new large signal LDMOS FET model in the design of a high power, UMTS band 60W Doherty amplifier. This new model will be shown to be capable of providing accurate predictions of power, gain, efficiency and most importantly, linearity of the complete amplifier.

1. Introduction

The design of low power (<10W) Doherty amplifiers at microwave frequencies using classical formulae to calculate the required output impedances has been well documented [1], [2]. The analysis has been extended to more complex topologies such as N-Way [3], [4]. Owing to the relatively low RF power levels and, therefore, the correspondingly low parasitic effects in the transistors the "classical" equations work well resulting in first time design success. This paper concentrates on the design of a 60W Doherty amplifier for the UMTS band (2.11GHz – 2.17GHz). When designing a Doherty amplifier at higher power levels it is important to realize that the impedances that must be matched for correct Doherty operation are no longer purely real, but have significant imaginary parts. An accurate large signal transistor model allows the achievement of first time design success. Preliminary work used a Spice-based model [5], which uses three basic components to model the devices' characteristic behavior. The three Spice elements are a MOSFET, a DIODE and a JFET. In simple terms the MOSFET models the turn-on region of the LDMOS device with the DIODE modeling vertical breakdown and the JFET modeling lateral channel breakdown. Whilst this model made excellent predictions of power, gain and efficiency (both at compression and at back-off) it was found to be insufficient in modeling the sub-threshold region for accurate predictions of backed-off linearity. In a Doherty amplifier it is even more critical that the sub-threshold regions be modeled accurately as the peaking amplifier (or amplifiers in an N-Way configuration) operates in this area of the I-V space being biased in Class B mode. This also implies that the small signal behavior is affected.

A new large signal model has been developed enabling the prediction of all aspects of the performance of the amplifier [6]. This model (called the CMC model) is based on the so-called 4-Region approach that accurately models the most important regions of the I-V space [7].

The same model has been exercised extensively in many different reference designs for Cree Microwave LDMOS transistors.

2. Amplifier Design

A 60W UMTS band Doherty amplifier, employing the packaged UGF21030 LDMOS FET, has been designed using the CMC large signal model to achieve good efficiency and linearity simultaneously. All large signal simulation work was performed in Microwave Office. Layout sensitive elements of the design were analyzed using Momentum. The design flow was as follows:

1. Development of the transistor level model
2. Single ended Circuit Modeling
3. Doherty Circuit Design
4. Manufacture and test of prototypes

The new CMC die model was developed by making extractions on a 1W test FET. This device has

the same layout as employed in the 30W transistor. The model coefficients were derived and the model checked against load pull and swept power measurements. A major feature of this new model is that it is scalable. The model was scaled to 30W and then the package model was developed. The first stage of package modeling was to make approximations of bond wire inductances including any mutual inductance effects. Next the package capacitances were calculated using simple parallel plate capacitor equations. With the complete package model in place the element values were then refined by comparing simulated data with measured s-parameter and load pull data.

The small signal s-parameter fits of the modeled UGF21030 transistor versus measured data over the frequency range of 0.5 to 3.0 GHz are shown in Figure 1. It can be seen that the fits are excellent over a broad bandwidth. The Smith chart plots of S11 and S22 show that the resonant frequencies of the input and output matches are well modeled. This was found to be of particular importance in achieving agreement with load pull data.

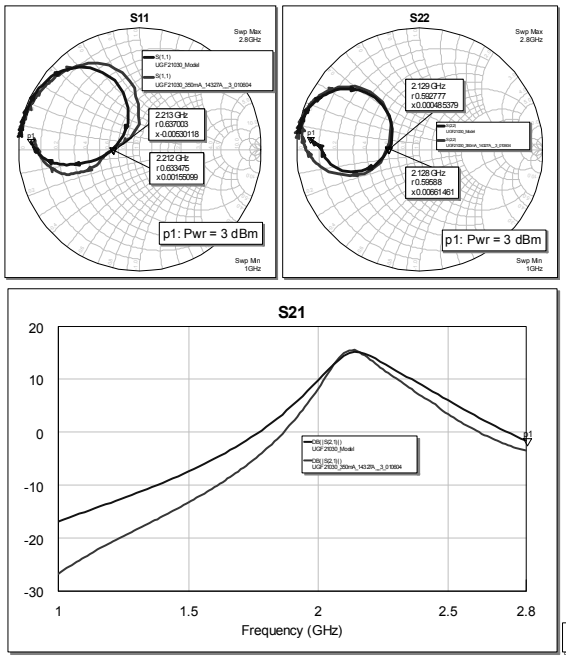

Figure 1. Fits to s-parameter data for UGF21030

The differences in S21 values between measurement and model with frequency are likely due to overly simplistic bond wire models. Figure 2 shows the simulated source and load pull results from the Microwave Office load pull wizard together with the optimum impedance points measured on an automated load pull system. Again good agreement can be observed. The performance of the UGF21030 model in terms of swept power was verified against data sheet curves.

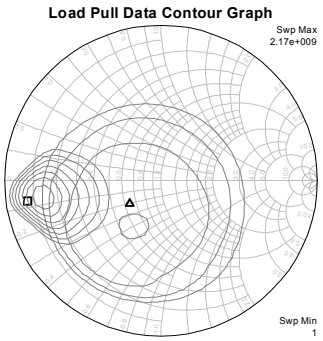

Figure 2. Fits to load and source pull data for UGF21030

Since the UGF21030 is a standard Cree Microwave product the 50 ohm test fixture design had already been completed so that the next step was to create models of the input and output matching networks. The complete Doherty amplifier circuit was then designed using these 50 ohm amplifiers as building blocks, adding the requisite additional phase lengths to enable transformations to the correct impedances [8]. The output matches of the carrier and peaking amplifiers were then tuned to give the best efficiency and linearity trade-off. The complete amplifier circuit was then load pulled to ensure that optimum performance had been achieved. The top-level circuit schematic can be seen in Figure 3.

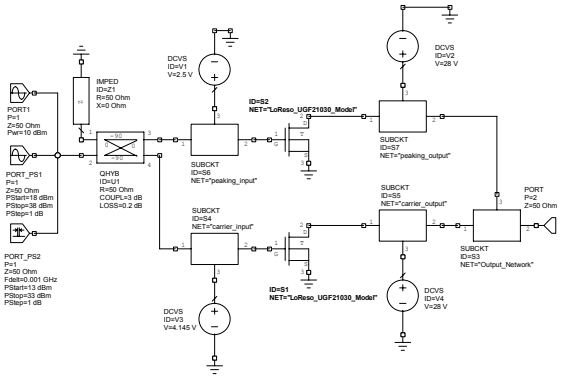

Figure 3. Complete Doherty Amplifier Model

The schematic shows three different input ports set up for convenience to allow all facets of the design to be looked at. The input and output matching blocks for the peaking and carrier amplifiers are all unique. They consist of microstrip elements and s-parameter blocks generated from the planar electromagnetic simulator. The input divider used was an Anaren Xinger, which is modeled as an ideal element with about 0.2dB loss. This was found to be sufficient for this work. It should

be noted that an s-parameter block may seem a more accurate alternative but the upper frequency of the available data files is 6GHz. This can be a source of error when performing harmonic balance simulations, as the higher order harmonics will be in an extrapolated region of the s-parameter data.

The circuit was realized using a 31mil thick, Teflon fiberglass board, which was sweat soldered to an aluminum plate for good grounding and heat sinking. The transistors were clamped into the circuit. The finished amplifier can be seen in Figure 4.

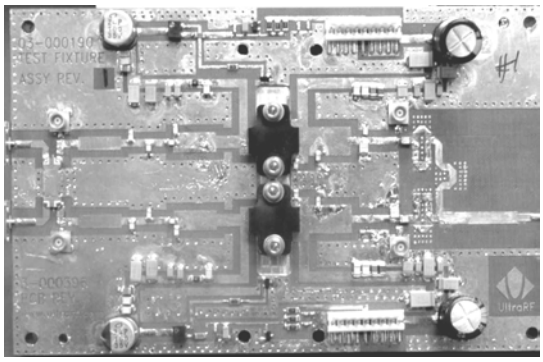

Figure 4. 60W Doherty Amplifier Prototype

3. Results

The 60W Doherty amplifier was evaluated under a number of different stimuli. The small signal gain of the amplifier was measured from 1.5GHz to 3GHz. A comparison of the measured and modeled results can be seen in Figure 5. The same frequency dispersion can be observed as with the transistor level model. The prediction of the nulls either side of the pass band is excellent. The upper null is attributable to the peaking amplifier. This implies that the transistor model works well, especially in the sub-threshold region.

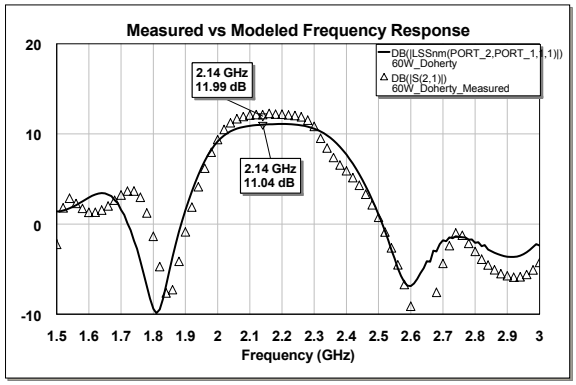

Figure 5. Small Signal Results

The amplifier has been measured over a 25dB dynamic range with gain, power and efficiency curves plotted simultaneously. These curves are presented in Figure 6. It is interesting to note that the efficiency curve, both modeled and measured, does not show a very strong Doherty shape. Without a model this may have been cause for concern as to whether the amplifier had been correctly implemented. It is however predictable and is a function of the high power level and linearity target.

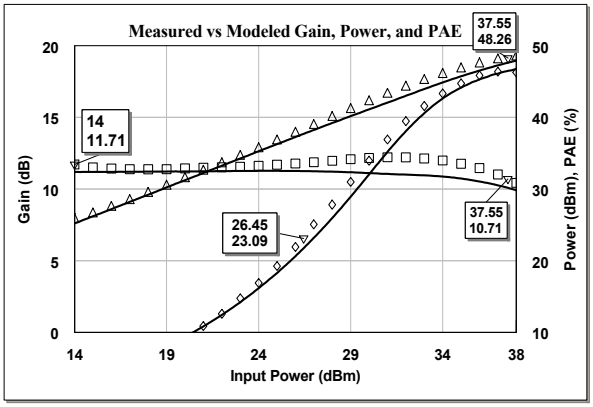

Figure 6. Large Signal Power Sweep

Swept power measurements were made using an Anritsu Power Amplifier Test System (PATS). The linearity of the amplifier was also measured using the PATS. The third, fifth and seventh order intermodulation distortion products were observed over 20dB of dynamic range. Data is presented in Figure 7. The prediction of the nulls in the responses is excellent.

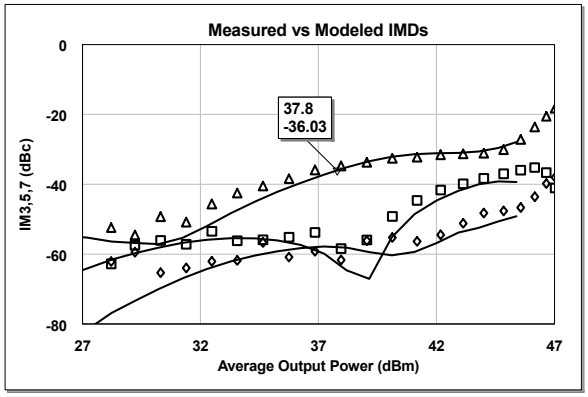

Figure 7. Intermodulation Results

Whilst this is a very fast measurement with all curves displaying simultaneously the system noise floor is compromised. This can be seen in the level of the IMD's at low power. The simulation has a superior noise floor predicting seventh order products down to more than -80dBc.

The amplifier was also evaluated under a two-carrier W-CDMA test signal and met an ACLR specification of –35dBc at 6W of average output power with a drain efficiency of 23%. The spectral plot is shown in Figure 8.

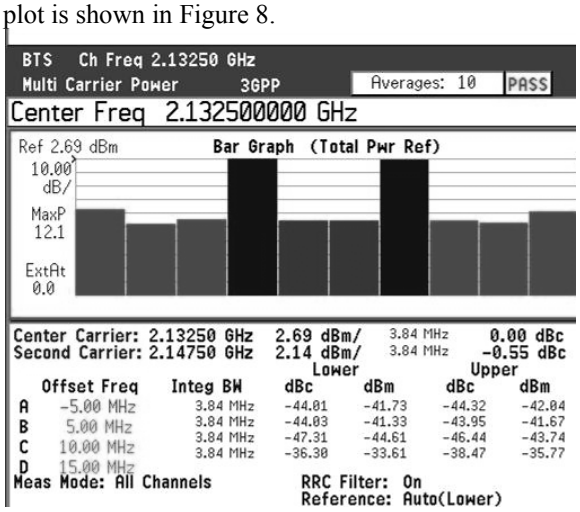

Figure 8. W-CDMA Result at 6W Average Output

4. Conclusions

A powerful new large signal model has been developed and demonstrated in a complex application that requires all regions of DC and RF operation to be well modeled. The results of this work show excellent agreement between simulations and measurements of the complete Doherty amplifier. Of considerable importance is the fact that the transistor model is capable of providing wide band simulations.

The model has provided further insight into the operation of higher power Doherty amplifiers and has highlighted some of the sensitivities of these designs. The number of variables in the Doherty amplifier makes practical tuning methods ineffective. Having an accurate large signal model allows the power amplifier designer to engineer more complex architectures with confidence.

5. Acknowledgements

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6. References

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