Highly Efficient Saturated Power Amplifier

Junghwan Moon, Juyeon Lee, Raymond S. Pengelly, Ryan Baker, and Bumman Kim

Junghwan Moon, Juyeon Lee, and Bumman Kim (jhmoon, davinch, bmkim}@postech.ac.kr) are with Department of Electrical Engineering and Division of Information Technology Convergence Engineering, Pohang University of Science and Technology (POSTECH), Pohang, Republic of Korea. Raymond S. Pengelly and Ryan Baker are with Cree Inc., Durham, NC, USA.

Prologue

The 7th Student High-Efficiency PA Design Competition was held at the International Microwave Symposium (IMS) 2011 in Baltimore, MD. Every year, many students from all over the world participate in the competition and demonstrate their ability to design a high-efficiency power amplifier (PA). Since IMS 2008, in order to encourage students to explore PA design at a high-frequency, a weighting factor was introduced to the calculation of the score - the final score being determined by multiplying the power–added-efficiency (PAE) by the frequency weighting factor, \( \text{PAE} \times (\text{frequency (GHz)})^{0.25} \). Thus, while preparing the competition, participants are encouraged to carefully determine the device technology considering the operating frequency of the PA as well as their high efficiency PA topology.

According to the competition rules, the PA is required to operate above 1 GHz but less than 20 GHz, and produces output power between 5 and 100 watts into a 50 Ohm load with maximum input power of 25 dBm. Therefore, minimum output power
should be greater than 37 dBm and the PA should have more than 12 dB power gain. To get high efficiency, the PA should be driven into its highly saturated region, requiring even higher gain at a high frequency. Among a number of device technologies, gallium nitride (GaN) high-electron-mobility transistors (HEMTs) are the most attractive candidates because they display lower parasitic capacitances than other technologies, delivering higher gain performance at frequencies higher than 3 GHz. After device selection, the proper class of operation should be considered. Various high-efficiency classes including switch-mode, such as the class-E and class-D, and harmonically tuned ones such as class-F and saturated PAs, have been extensively investigated to find the best solution for the highest efficiency from the given device technology. Among the classes, harmonically tuned PAs are preferred at the higher frequencies because true switching operation is more difficult to achieve, resulting in lower efficiencies.

In this article, we summarize the design procedure of the winning PA at the 2011 IMS Student Design Competition. The circuit topology of the winning amplifier is based on the saturated PA [1]–[3]. At an operating frequency of 3.475 GHz, this amplifier delivers an output power of 38.4 dBm and a PAE of 80.1%, which is equivalent to a weighted score of 109.16, with an input power of 24 dBm, a drain supply voltage of 28 V, and idle current of 50 mA. Our group was also awarded the
first prize in 2008 using the same saturated PA approach [1], but for our 2011 PA we paid more attention to detailed design optimization.

**Waveform Engineering for High Efficiency**

The key point for high-efficiency operation lies in the output waveform engineering, in which the overlap between the voltage and current is minimized, reducing the power dissipation in the transistor and thus improving the efficiency [1]–[5]. Figure 1(a) shows the optimum candidates of the voltage and current waveforms for the high-efficiency PA, that is, half sinusoidal and rectangular shapes. For the current, the maximum value is limited by the saturated current level of the transistor. Since the transistor acts as a voltage controlled dependent current source, the current waveform is determined mainly by input voltage and device physical limitations such as pinch-off and saturated characteristics. Thus, infinite harmonic contents are included in the current waveform. On the other hand, the voltage waveform is shaped by the current and load impedance. Practically, only a few harmonics, normally up to the third, can be manipulated. That is, the infinite harmonic loading circuit is not feasible, and the voltage waveform is composed of finite harmonic content, that is, DC, fundamental, second, and third harmonic components as shown in Figure 1(b). The half-sinusoidal waveform is formed by the fundamental
component assisted by the out-of-phase second harmonic component with amplitude of $V_1/6$ and the rectangular waveform by the fundamental component assisted by the out-of-phase third harmonic component with amplitude $V_1\sqrt{2}/4$, where $V_1$ means the fundamental voltage. Since the efficiency is calculated by the fundamental output power divided by the DC power, the waveform with a large ratio of the fundamental to DC components is preferred for high efficiency. At a glance, the PA with the half-sinusoidal current and voltage waveforms would be the best choice for high efficiency operation [4], [5]. However, in this case, the efficiency exceeds 100%, that is, 111%, indicating that the waveform cannot be generated.

$$\eta = \frac{P_1}{P_{DC}} = \frac{1}{2} \frac{V_1 \cdot I_1}{V_{DC} \cdot I_{DC}} = \frac{1}{2} \frac{\sqrt{2} \cdot \frac{1}{2}}{\frac{1}{\pi} \cdot \frac{1}{\pi}} = \frac{\sqrt{2}}{4} \cdot \pi = 111\% \tag{1}$$

$I_1$ represents the fundamental current. Such a waveform can be obtained with the negative second harmonic load. This negative impedance means that the external second harmonic power should be excited because the passive circuit cannot make the negative impedance. To eliminate the negative second harmonic load, the voltage waveform should be moved by at least 45 degree with the complex fundamental and capacitive second harmonic loads, as shown in Figure 1(c). In this case, there is some overlap between the fundamental voltage and current waveform, but the half sinusoidal voltage and current waveforms can be maintained, which has become...
known as the class-J amplifier. Due to the overlap between the waveforms, the class-J amplifier dissipates power internally and reduces the power and efficiency, resulting in the same efficiency as class-B amplifiers [2], [4].

The half sinusoidal current and the rectangular voltage and its “dual” PA can deliver efficiencies of 100%, which are so-called class-F and class-F\(^{-1}\), respectively. As mentioned earlier, the saturated amplifier, we are using in this paper, has a quasi-rectangular current waveform and a quasi-half-sinusoidal voltage waveform described in Figure 1(b), which is the waveforms of class-F\(^{-1}\) amplifier. The voltage and current waveforms are shaped using the self generated harmonic components [2]. Since the output capacitor in the transistor is highly nonlinear, the capacitor generates a large amount of second harmonic voltage with a few higher order harmonics. Thus, the self-generated harmonic voltage assists in forming the quasi-half sinusoidal voltage, which will be described later. The harmonic voltages can be large enough when the PA is driven by the large input power with a large fundamental load. In this drive condition, the current becomes the quasi-rectangular shape by the bifurcated current in the saturated operation. Thus, the efficiency of the PA can approach 90% [2], [3], [5]. In the remainder of this article, we will explain the operational behavior of the saturated PA, and describe the implementation method and experimental results of the winning PA.
Waveform Shaping Method of Saturated PA:

Harmonic Generation of Nonlinear Output Capacitor

Figure 2 shows a simplified circuit diagram of the saturated amplifier. As mentioned previously, the saturated amplifier utilizes the harmonic voltages generated by the nonlinear output capacitor, $C_{OUT}$, for voltage waveform shaping. In high frequency model, $C_{OUT}$ is sum of $C_{DS}$ and $C_{GD}(1-1/A_v)$ by Miller effect. The harmonic voltages from the $C_{OUT}$ consist of a large second harmonic component with smaller higher order harmonics. Thus, the half-sinusoidal shaped voltage across the capacitor can be generated easily using large harmonic loads [2], [3], [5].

To demonstrate the harmonic generation by the nonlinear $C_{OUT}$, we have investigated the simplified circuit in Figure 2, where the nonlinear behavior of $C_{OUT}$ is depicted in Figure 3. $C_{OUT}$ is extracted from large signal model provided by Cree. Figures 4(b) and (c) show the simulation results of the circuit with the sinusoidal current source shown in Figure 4(a). The simulation is carried out by both Agilent Advanced Design System (ADS) and AWR Microwave Office (MWO) using Cree’s large signal model. The simulation results include the voltage waveforms generated by the linear and nonlinear $C_{OUT}$ in the time-domain and frequency-domain.

Differently from the linear capacitor, the nonlinear capacitor generates a voltage
waveform consisting of the fundamental and a large second-harmonic component with small higher-order components even though only the fundamental current is injected into the capacitors. We have reported the same phenomenon for the real device case with the saturated current source, which has large second and third harmonic currents [3]. These results indicate clearly that the nonlinear \( C_{\text{OUT}} \) is the main source of the second harmonic voltage. The voltage across the capacitor is proportional to the integral of the current through the \( C_{\text{OUT}} \), the charge in the capacitor, scaled by the capacitance. It can be expressed by

\[
V_{DS}(t_x) = V_{DD} + \frac{1}{C_{\text{OUT}}(V_{DS}(t_x))} \int_{t_x}^{\infty} i(t) dt = V_{DD} + \frac{Q(t_x)}{C_{\text{OUT}}(V_{DS}(t_x))}
\]

(2)

where \( Q(t_x) \) is the accumulated charge on \( C_{\text{OUT}} \) until \( t_x \). When \( Q(t_x) \) decreases with negative \( i(t) \), \( V_{DS}(t_x) \) decreases and so \( C_{\text{OUT}} \) increases rapidly. When the voltage is near its minimum value, the output voltage \( V_{DS}(t_x) \) cannot change much because of the large increase of the \( C_{\text{OUT}} \) with the limited current drive. That is, \( Q(t_x)/C_{\text{OUT}}(V_{DS}(t_x)) \) remains nearly constant around that region. As a result, the voltage waveform has a flattened bottom in the low voltage region, like the half-sinusoidal shape, as shown in Figure 4(b). To get the voltage waveform, as show in Figure 1(b), in which the fundamental voltage is \( \sqrt{2} \) times larger than that of the sinusoidal waveform, the fundamental load should be about \( \sqrt{2} \) times larger than the conventional case and the second harmonic load should be tuned appropriately.
To demonstrate the operation of the saturated amplifier with a real device, the amplifier is simulated using Cree’s GaN HEMT CGH60008D bare-die large signal model at 3.5 GHz. All simulations are carried out by ADS and MWO. Figure 5 shows the harmonic load-pull contours. Simulation results clearly show that the saturated amplifier delivers high efficiency for the broad high impedance levels of harmonic loads, verifying the harmonic generation of the nonlinear $C_{OUT}$, and such high efficiency can be obtained even at the highest frequency. The resultant voltage and current waveforms of the saturated amplifier are depicted in Figure 6, which is quite similar to the waveforms in Figure 1(b). As mentioned previously, the saturated amplifier delivers the half sinusoidal voltage waveform along with the quasi rectangular current shape.

**Implementation of Saturated PA**

To design a high efficiency PA at a frequency of 3.5 GHz, the saturated PA, explored in the previous section, has been designed using Cree’s GaN HEMT CGH60008D bare chip model. This amplifier employs the nonlinear output capacitor with proper second harmonic load to shape the voltage waveform. Due to the saturated operation of the PA, the current waveform is bifurcated, resulting in the quasi rectangular current shape with a large third harmonic current. The simulation
results using the bare-chip model verify the operational behavior of the PA including the voltage shaping of the nonlinear capacitor [1].

A saturated amplifier was designed and implemented at 3.5 GHz using Cree’s GaN HEMT CGH40006P packaged model, including CGH60008D bare-chip and package elements. Although the nonlinear output capacitor generates the half-sinusoidal voltage waveform, we have already highlighted the importance of the second harmonic load to obtain the optimal half-sinusoidal waveform. Thus, to find the proper load conditions for the fundamental and harmonics, the load-pull simulation is carried out using the packaged model, and its result is depicted in Figure 7. Compared to the result of the bare-chip model, the tolerance of the harmonic loads for the efficiency is reduced due to the package elements such as bonding wire and lead capacitor. However, since the optimum second and third harmonic loads for the high efficiency are located near the short impedance level, the matching for the harmonics can be realized using a simple open stub or at the bias line. On the other hand, we have found that the harmonic match at the source has a large tolerance for high efficiencies [2]. Based on the source/load-pull simulation results, the targeted load impedances at the fundamental, second harmonic, and third harmonic frequencies are set to $(8.647+j20) \, \Omega$, $0 \, \Omega$, and $0 \, \Omega$, respectively. For the source network, the fundamental source impedance is set to $(3.613-j8.949) \, \Omega$. 


while all input harmonics are short circuited.

Based on the impedances found by the source/load-pull simulation, the saturated PA was designed and implemented at 3.5 GHz. Figure 8 shows the schematic diagram of the saturated amplifier and Figure 9 depicts the photo of the amplifier, which is the winning PA at the 2011 IMS Student Design Competition. Since the harmonic source impedances have negligible effects on the efficiency, the input circuit is matched only for the fundamental component. On the other hand, the harmonic load impedances are crucial for the high efficiency of the saturated amplifier. For the proper terminations of the second and third harmonics, which are short circuits, the three transmission lines are employed, where TL₀₁ and TL₀₂ are used for the short circuit of the second harmonic, and TL₀₁ and TL₀₃ for the short circuit of the third harmonic. The input and output matching networks are optimized to deliver the highest efficiency at 3.5 GHz using the Momentum simulator.

**Experimental Results**

Figure 10 shows the measured and simulated small signal gain performance of the implemented saturated amplifier with a drain-source voltage of 28 V and an idle current of 50 mA. The measured small signal gain is well matched to the simulated one. Figure 11 shows the measured and simulated CW performance at
3.475 GHz and 3.5 GHz. Initially, the saturated amplifier was designed at 3.5 GHz. However, fabrication errors during the implementation such as changes of the width and length of the transmission line lead to the frequency shift to 3.475 GHz. Moreover, the Momentum simulation is a time-consuming task so that optimization for the matching circuit was not carried out thoroughly. The measured gain characteristics for both frequencies are higher than those of the simulation results. However, good agreement between the measured and simulated results was achieved at the high power level. In the experiment, a peak PAE of 80.1% is measured at 3.475 GHz with an output power of 38.4 dBm and a power gain of 14.4 dB. Figure 12 shows the measured and simulated output power, gain, drain efficiency, and PAE performances across a frequency band for a constant input power of 24 dBm. The saturated amplifier delivers above 70% PAE across 150 MHz frequency band. The measurement results clearly show that the saturated amplifier is suitable for a high efficiency PA at a high operating frequency.

**Conclusions**

In this article, a high-efficiency saturated amplifier has been presented. This amplifier takes advantage of the nonlinear output capacitor to shape the voltage waveform. The nonlinear capacitor generates substantial second harmonic voltage
with small higher order harmonics. Thus, using $\sqrt{2}$ times larger fundamental load and
the proper second harmonic termination, the resultant voltage waveform can be half-
sinusoidal. For high efficiency, the PA should be driven by the large input power.
Therefore, the current of the PA is bifurcated, resulting in the quasi- rectangular
current shape. The resultant output waveforms are similar to those of class-F\(^{-1}\)
amplifiers, whose waveforms are optimal for high efficiencies. Based on harmonic
source/load-pull simulation, the saturated amplifier has been designed using Cree’s
GaN HEMT CGH40006P packaged model. The matching networks for the input and
output were optimized using the Momentum simulator. The implemented amplifier
delivered a PAE of 80.1% at 3.475 GHz. The simulation and measurement results
verify that the saturated amplifier is suitable for a high-efficiency PA over a relatively
high frequency band.
Acknowledgment

This work was supported by the MKE (The Ministry of Knowledge Economy), Korea, under the ITRC (Information Technology Research Center) support program supervised by the NIPA (National IT Industry Promotion Agency) (NIPA-2010-(C1090-1011-0011)) and WCU (World Class University) program through the Korea Science and Engineering Foundation funded by the Ministry of Education, Science and Technology (Project No. R31-10100).

The authors would like to thank Cree Inc., Durham, NC, USA for providing the GaN HEMT transistors and large signal models used in this work.
References


Figure Captions:

Figure 1. Candidates of current and voltage waveforms for high-efficiency PA. (a) Current waveforms with infinite harmonics. (b) Voltage waveforms with up to third harmonics. (c) Waveforms of the saturated PA and class-J amplifier.

Figure 2. Simplified circuit diagram of the saturated PA.

Figure 3. Nonlinear behavior of the output capacitor.

Figure 4. Harmonic generation properties of the linear and nonlinear output capacitors. (a) Current flowing through the capacitor. The resultant voltages across the capacitors in the (b) time- and (c) frequency-domains.

Figure 5. Harmonic load-pull contours of CREE GaN HEMT CGH60008 bare-die model at 3.5 GHz: (a) fundamental, (b) second harmonic, and (c) third harmonic. In this loadpull, the other impedances are the optimum values. Blue and red lines represent the output power and PAE, respectively. Figure 6. Simulated drain-source voltage and current waveforms of the saturated PA when the PA is driven by the constant input power of 25 dBm. During the simulation, the load impedances for fundamental, second harmonic, and third harmonic are set to 19.467+j39.049, 1.1+j23.744, and 0.308+j23.744, respectively. The fundamental source impedance is set to 3.613+j8.949 while all input harmonics are shorted.

Figure 7. Harmonic load-pull contours of CREE GaN HEMT CGH40006 packaged...
device model at 3.5 GHz: (a) fundamental, (b) second harmonic, and (c) third harmonic. Blue and red lines represent the output power and PAE, respectively.

Figure 8. Circuit topology of the saturated PA at 3.5 GHz.

Figure 9. Photo of the implemented PA.

Figure 10. Measured and simulated small signal gain of the implemented saturated PA.

Figure 11. Measured and simulated CW performance at (a) 3.475 and (b) 3.5 GHz.

Figure 12. Measured and simulated performance across the frequency for a constant input power of 24 dBm.
Figure 1.

(a) 

\[ I_{DC} = \frac{I_{MAX}}{\pi} \]
\[ I_1 = \frac{I_{MAX}}{2} \]
\[ I_1/I_{DC} = \frac{\pi}{2} \]

(b) 

\[ V_{DC} = \frac{V_{DC}}{2} \]
\[ V_1 = \sqrt{2} V_{DC} \]

(c) 

Class-J
Saturated PA

\[ I_{DC} : \text{DC component of current} \]
\[ I_1 : \text{fundamental component of current} \]
\[ V_{DC} : \text{DC component of voltage} \]
\[ V_1 : \text{fundamental component of voltage} \]

Figure 2.

\[ V_{DD} \]
\[ I_{DS} \]
\[ Z_{Load} \]


This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of Cree’s products or services. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permissions@ieee.org. By choosing to view this document, you agree to all provisions of the copyright laws protecting it.
Figure 3.

![Figure 3](image.png)

**Figure 4(a).**

![Figure 4(a)](image.png)

**Figure 4(b).**

![Figure 4(b)](image.png)
Figure 4(c).

![Graph showing Capacitor Voltage (V) vs Frequency (GHz) for Linear and Nonlinear Capacitors.]

Figure 5(a).

![Graph showing power levels (dBm) and efficiency percentages.]


This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of Cree’s products or services. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permissions@ieee.org. By choosing to view this document, you agree to all provisions of the copyright laws protecting it.
Figure 5(b).

Figure 5(c).
**Figure 6.**

Input power of 25 dBm

**Figure 7(a).**

40.2 dBm
39.2 dBm
38.2 dBm
37.2 dBm
36.2 dBm

81.5%
77.5%
73.5%
69.5%
65.5%
Figure 8.

Figure 9.
Figure 10.

![Small Signal Gain vs Frequency](image)

- Measurement
- Simulation

Figure 11 (a).

![Output Power, Drain Efficiency, PAE vs Input Power](image)

3.475 GHz, $V_{DS} = 28$ V, $V_{GS} = -2.7$ V ($I_{DSQ} = 50$ mA)

Filled : Measurement  
Hollow : Simulation  

Output Power, Gain, Drain Efficiency, PAE vs Input Power (dBm)
Figure 11 (b).

3.5 GHz, $V_{DS} = 28$ V, $V_{GS} = -2.7$ V ($I_{DSQ} = 50$ mA)

Filled : Measurement
Hollow : Simulation

Output Power (dBm), Gain (dB)

Figure 12.

$V_{DS} = 28$ V, $V_{GS} = -2.7$ V ($I_{DSQ} = 50$ mA), $P_{in} = 24$ dBm

Filled : Measurement
Hollow : Simulation

Gain

Drain Efficiency

PAE

Output Power (dBm), Gain (dB)

Frequency (GHz)