Two-Stage Ultrawide-Band 5-W Power Amplifier Using SiC MESFET

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Abstract— This paper describes a two-stage 5-W broad-band amplifier covering the frequency range from 10 MHz to 2.4 GHz. An SiC MESFET is used as the power stage. A large-signal table-based model has been developed and verified for the SiC device by comparison with measurements. A novel broad-band choke structure was developed to obtain high dc isolation and low RF loss over the full bandwidth. No impedance transformer was used at all. Broad-band input and output matching networks and shunt feedback topology were introduced to fulfill the bandwidth requirements. Typical values of 22-dB power gain, 37-dBm output power, 28 % power-added efficiency and 47-dBm third-order intercept points have been achieved in a two-stage design using a GaAs MESFET as driver stage. All power and linearity results were obtained over the whole frequency band. The design procedure is given in detail and the results are being discussed and compared with simulations.

Index Terms —MESFET, silicon carbide, table-based model, two-stage power amplifier (PA).

I. INTRODUCTION

FEATURES of wide-bandgap semiconductors that provide high RF power density [1], excellent power-added efficiency (PAE) performance, high breakdown voltage, high-frequency operation, small die size, and less complex amplifier arrangement make such technology a serious challenge to silicon LDMOS devices for high-power applications [2]−[4]. Over the last years, many authors have utilized these superior features of SiC MESFETs and have applied them in the development of different generations of power amplifiers (PAs) for use in digital audio and video broadcasting [5], [6] and aerospace and military systems [7]−[9]. A comparison of Si, GaAs and SiC MESFET power densities indicates, that SiC is a very promising material for high-power and high-frequency operation [10]. A serious problem of wide-band PAs, especially in the GaAs field effect transistor (FET) and GaAs monolithic-microwave integrated-circuit (MMIC) cases [11], [12] is the output matching because of the low intrinsic device impedance. Depending on the amplifier data, this problem can be mostly overcame only by using (external) transmission-line transformers that strongly limit the total bandwidth. The SiC-MESFET technology avoids this drawback and provides high large-signal output impedance because of its high drain−source breakdown voltage. In hybrid arrangements, as in this study, the advantages of GaAs and SiC can be combined successfully. As a first step, we have introduced an ultra-broad-band SiC MESFET 5-W single-stage PA in [13]. In this paper, we discuss modeling aspects, present enhanced results and an extension toward a two-stage
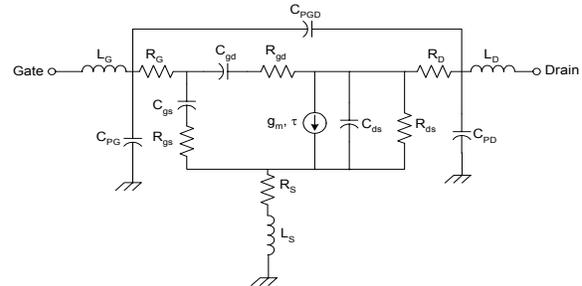

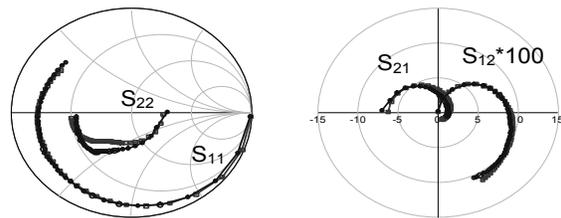Fig. 1.   Small-signal equivalent circuit.

Fig. 2.   Simulated and measured S-parameters at V_{DS} = 30 V and V_{GS} = –9 V from 1 MHz to 4 GHz. squares: measurements, circles: simulations.

design as a continuation of the previous study. For the first time, the two-stage amplifier provides 5-W output power and 22-dB power gain within a frequency range from 10 MHz to 2.4 GHz without any kind of impedance transformer.

Section II describes in brief the modeling work performed for the SiC MESFET. It is an extension of the results given in [14] toward large-signal modeling.

Section III introduces the design procedure in three steps. First, the selection process leading to the power transistor, which fulfills the design requirements, is described. The development of the dc-biasing networks that meet the desired bandwidth is considered in the next step, while the third one deals with input, output, and interstage matching networks (ISMNs), as well as shunt feedback circuit design resulting in the required broadband characteristic.

In Section IV, experimental results are given and discussed. Small-signal gain, stability factor, and matching, as well as power performance measurements (PAE, output power, and power gain) over the frequency range from 10 MHz to 2.4 GHz are introduced. Two-tone measurements with frequency spacing of 200 kHz and AM–AM and AM–PM conversion data followed by noise figure (NF) measurements are also carried out, and the influence of the driver stage on the overall
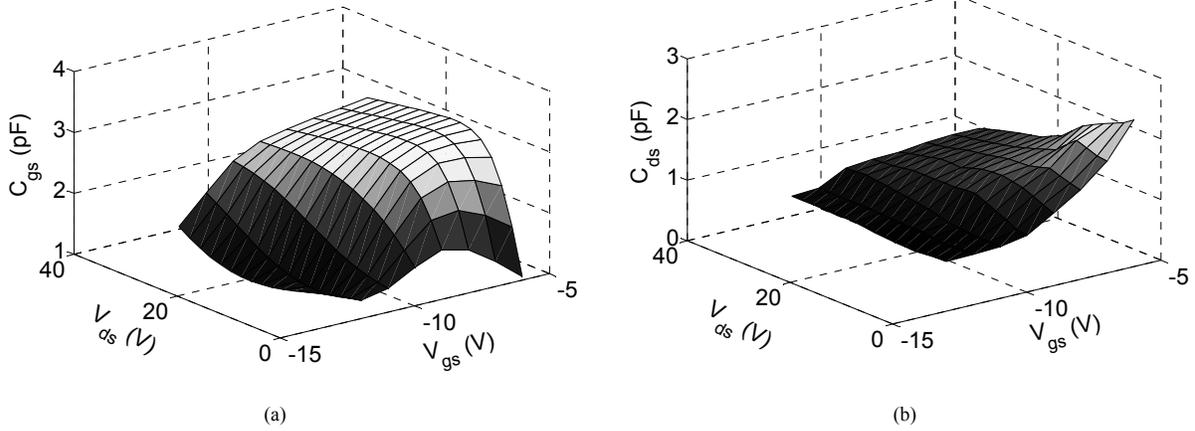
Fig. 3.   Modeled: (a) C_{gs} and (b) C_{ds} as a function of internal control voltages.

performance is discussed. Finally, the design procedure and experimental results are concluded in Section V.

II. SiC MESFET MODELING

The modeling work done for the SiC MESFET is described in brief here. Numerical values are related to the CREE CRF-24010 device. Fig. 1 shows the small-signal equivalent circuit used.

The model elements are divided into two categories, i.e., the extrinsic parasitic elements (R_S, R_G, R_D, L_S, L_G, L_D, C_{PG}, C_{PD} and C_{PGD}) and the intrinsic bias-dependent elements (C_{gs}, C_{gd}, C_{ds}, R_{gs}, R_{gd}, R_{ds}, g_m, and τ).

Note that the extrinsic parameters are capital letter subscripted, while subscripts in small letters denote the intrinsic parameters.

The parasitic elements were extracted using a cold-FET technique as reported in [14]. The initial values of some intrinsic elements (R_{ds}, g_m, and τ) were evaluated according to the procedure given in [16]. The other initial parameters were estimated from experience. Finally, an optimization process was applied, resulting in a minimum error function. As a result, good agreement was found between measured (squares) and simulated (circles) S-parameters (Fig. 2). The deviation in S_{22} was analyzed and a network analyzer calibration problem has been found as a real cause.

Other selected examples concerning the small-signal model at multiple bias points are given in Fig. 3 for the intrinsic capacitors C_{gs} and C_{ds}.

Concerning the large-signal behavior of the SiC-MESFET, the Angelov model [15], [17] has been found to be a very suitable base. We achieved accurate results for both dc and harmonic-balance simulations with minor changes and extensions of the model equations. Fig. 4 shows a comparison of simulated and measured output characteristics of the used transistor and good agreement can be noticed.

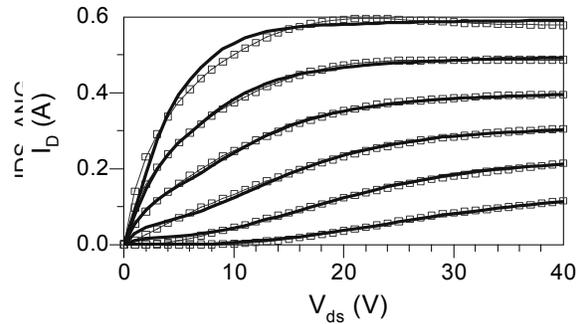The proposed model has been implemented as a user-defined model into the harmonic-balance circuit

Fig. 4.   Measured (squares) and simulated dc output characteristics. V_{gs} varies from –11 V to –6 V.
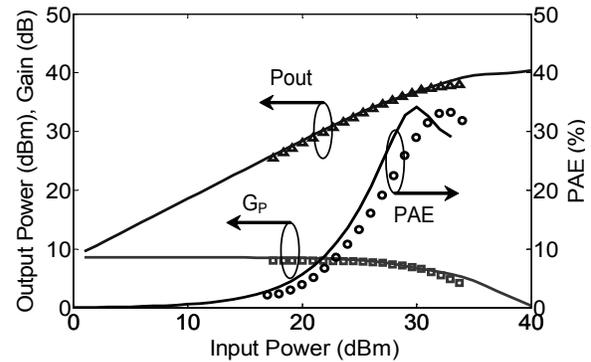

Fig. 5.   Measured (symbols) and simulated (solid lines) power performance of a single-stage PA based on the derived model. $f = 1$ GHz, $V_{DS} = 30$ V, and $I_D = 500$ mA.

simulator ADS from Agilent and small- and large-signal simulations were accomplished.

Simulated output power, gain compression, and power-added efficiency of the SiC power stage based on the derived model have been compared with measurements. Fig. 5 shows the results at $f = 1$ GHz, $V_{DS} = 30$ V, and $I_D = 500$ mA. A very good agreement concerning power gain and output power can be observed, whereas the PAE curves show a slight difference.

The impact of case temperature variation has also been studied, and the temperature model has been verified this way. Fig. 6 shows the simulated and the measured power
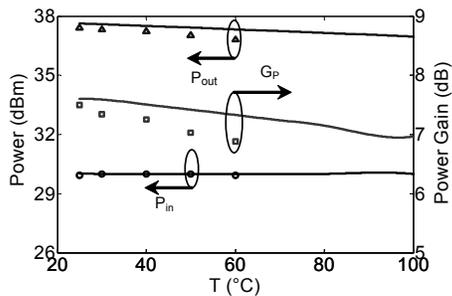

Fig. 6.   Measured (symbols) and modeled (solid lines) power-stage performance versus case temperature. $f = 1$ GHz, $V_{DS} = 30$ V and $I_D = 500$ mA.
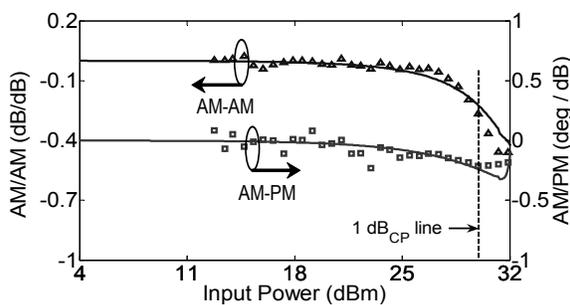

Fig. 7.   Measured (symbols) and modeled (solid lines) AM–AM (triangles) and AM–PM (squares) conversions of the SiC MESFET power stage; $f = 2$ GHz, $V_{DS} = 30$ V, and $I_D = 500$ mA.

performance of the SiC power stage versus case temperature. A good agreement between simulations and measurements has been achieved with only 0.6-dB deviation of the power gain at 60 °C.

Single-tone linearity performance of the derived model has been studied on the base of AM–AM and AM–PM response. AM–AM distortion is created by variation of the amplifier gain as a function of input power, while AM–PM distortion is defined as change of the phase between input and output signals with varying input power. Mathematically, AM–AM and AM–PM distortions are defined by

$$AM - AM = \frac{\partial G_P}{\partial P_{in}} \qquad (1)$$

$$AM - PM = \frac{\partial \phi(G_P)}{\partial P_{in}} \qquad (2)$$

where $\phi(G_P)$ is the transmission phase in degrees. Fig. 7 shows the measured and simulated AM–AM and AM–PM conversions of the power stage at 2 GHz. The AM–AM response has a compression characteristic, which is rather soft with only 0.3 (decibels per decibel) at 1 dB$_{CP}$. The AM–PM response shows a similar weak behaviour with only 0.2 (degree per decibel) changes at 1

dB$_{CP}$. The figure also shows an excellent agreement between simulations and measurements.

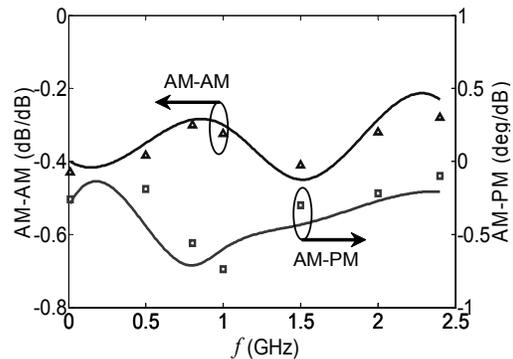Measured and simulated AM–AM and AM–PM

Fig. 8.   Measured (symbols) and modeled (solid lines) AM–AM and AM–PM response of the SiC power stage versus frequency. $V_{DS} = 30$ V, and $I_D = 500$ mA.
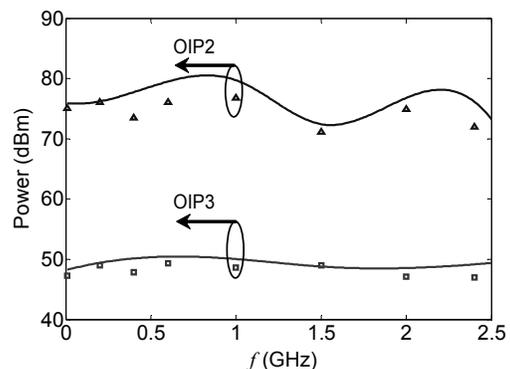

Fig. 9.   Measured (symbols) and simulated (solid lines) IP2 and IP3 of the SiC power stage versus frequency. $\Delta = 200$ kHz, $V_{DS} = 30$ V, and $I_D = 500$ mA.

distortions have been extracted over the entire bandwidth and depicted in Fig. 8 at 1 dB$_{CP}$. The figure shows a very satisfying agreement between measurements and model-based simulations with only a few percent deviation. Very low values for AM–AM and AM–PM distortions of 0.45 (decibel per decibel) and 0.75 (degrees per decibel), respectively have been achieved over the full band at 1 dB$_{CP}$.

Measured and simulated second- and third-order intercept points of the SiC power stage using a tone spacing $\Delta = 200$ kHz are depicted in Fig. 9. Output second-order (IP2) and third-order intercept-point (IP3) values of higher than 70 and 47 dBm, respectively, have been achieved. Typically, the predictions are too optimistic by a few dBm.

III. DESIGN

A. Transistor Choice

The first and most important step in a PA design process is the selection of a suitable transistor for the

power stage in order to meet the required specifications of the amplifier. In this study, the design goals were a wide frequency range from 10 MHz to 2.4 GHz with a considerably flat small-signal gain of $\geq 23 \pm 1$ dB and an output power of at least 5 W. Due to the power requirements and the limited operating voltage of LDMOS and HBT devices, broad-band impedance transformation would be necessary by using such devices. This is a serious drawback because ultra-broad-band impedance transformation is complicated and lossy.
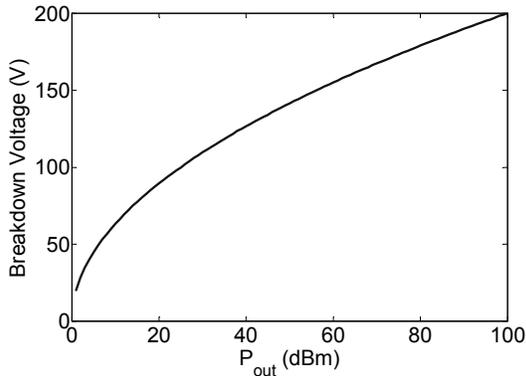

Fig. 10. Breakdown voltage of the power stage versus output power required for a 50-Ω load.
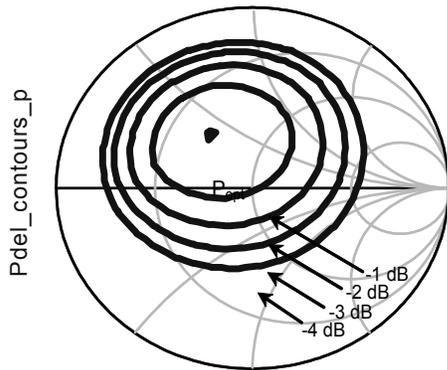

Fig. 11. Output power contours based on load–pull simulations (step-1 dBm) at 2.4 GHz.

The tradeoff between output power and required drain–source breakdown voltage V_{br} of the power FET is based on (3), given for an inductive-fed class-A power stage

$$V_{br} = \sqrt{8 P_{out} R_L} \tag{3}$$

The knee voltage of the FET is neglected in this first-order approach. Based on (3) and by using a 50-Ω load, the required V_{br} is depicted in Fig. 10 versus the output power.

Due to the high bandgap of SiC, FET devices based on this material system are able to operate up to more than 100-V drain–source voltages and, therefore, are able to match 50-Ω loads (at low frequencies) up to a few tens of watts without additional impedance transformation.

Therefore, the CREE CRF-24010 SiC MESFET device has been selected as power stage for our application. It is specified for applications up to 3 GHz and 10 W of output power. A small-signal gain up to 15 dB is achievable. Numerical load–pull optimization has been performed at the highest frequency to indemnify the 5-W output power at 2.4 GHz. In our broad-band application, load–pull characterization at lower frequencies is less important because the optimum load impedance is not sustainable over the full bandwidth and, on the other
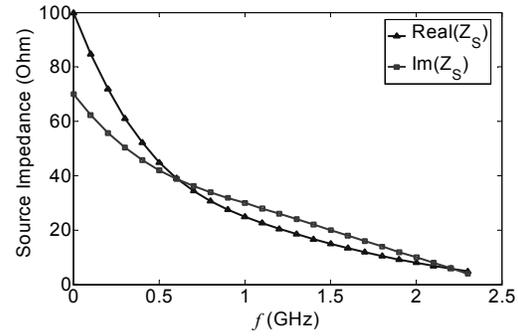

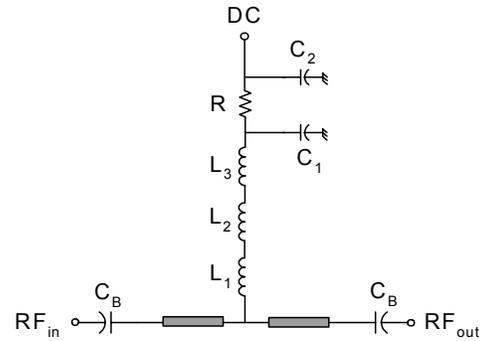
Fig. 12. Optimum source impedances versus frequency.

Fig. 13. DC-biasing network.
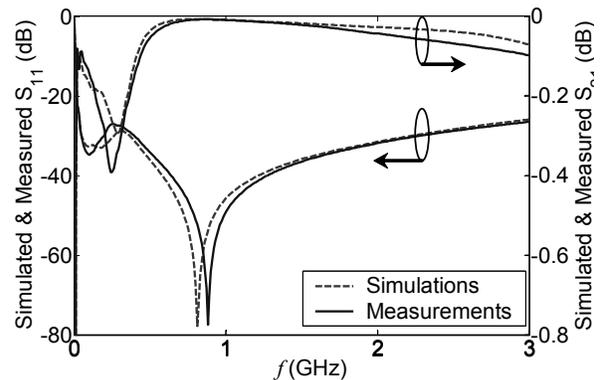

Fig. 14. Simulated and measured S-parameters of the broad-band choke for the power stage.

hand, power requirements at lower frequencies also become more and more relaxed. The simulated load–pull data at 2.4 GHz are shown in Fig. 11.

At 1-dB power compression, a maximum output power of 38.8 dBm at 2.4 GHz was found for optimum load and source impedances at the same time. This proves that the SiC device works close to its limit in our design at the high-frequency end. Optimal load impedance was found to be nearly real (37 Ω) and very weak, dependent on frequency. In contrast, the source impedance shows strong dependence on frequency (Fig. 12).

Optimum source and load impedances of the SiC device at 2.4 GHz, as well as power flatness over the full band were the design goals for the broad-band matching

Good agreement between simulated and measured results can also be observed.

C. Feedback and Matching Networks

In broad-band amplifier design, Darlington technique, based on two transistors shunted with a feedback resistor, has been presented and modified by Armijo and Meyer [20]. This technique suffers from PAE reduction because the transistors do not saturate at the same time. Krishnamurthy et al. [21] has improved this approach by
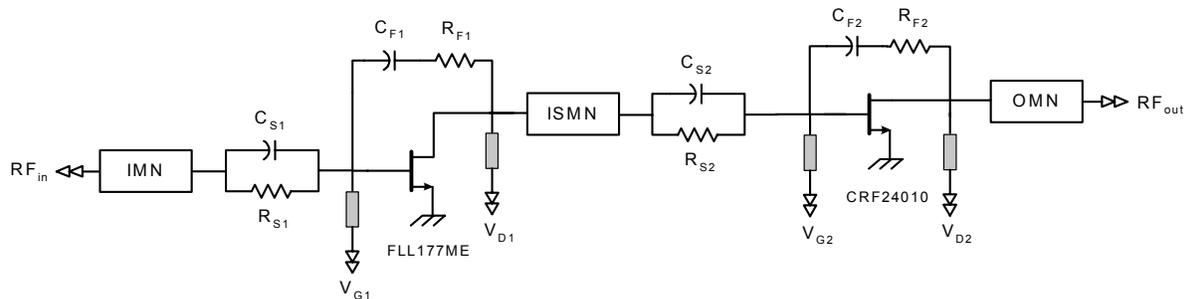

Fig. 15.   Two-stage PA structure.

networks described in Section III-C.

For the driving stage, a GaAs FET (Fujitsu FLL177ME) with the following specifications has been used:

- output power at 1 $dB_{CP} \approx 32.5$ dBm;
- small-signal gain ≈ 12.5 dB at 2.3 GHz.

B. DC-Biasing Network

The chokes have to be designed very carefully because they influence frequency response and stability of the amplifier. Very large inductance values have to be realized because of the low corner frequency of 10 MHz. The inductance has been split up into three series-connected elements of different size to overcome the problems with parasitic capacitive coupling. Thus, a sufficiently high self-resonance frequency (SRF) [18] has been obtained. Air- and ferrite-loaded coils have been used and tested using an evaluation board. Reflection and transmission coefficients of the chokes have been measured and optimized this way.

The three coils in combination with a small resistor in between two parallel bypass capacitors have been found as a suitable solution (see Fig. 13). The capacitance values C_1 and C_2 are selected to give very low reactance over the whole operating frequency range. Together with the low-impedance resistor, they are also responsible for supporting absolute stability over the whole operating range of the amplifier. The dc blocking capacitors (C_B) have to provide a good RF through over the whole bandwidth.

Fig. 14 shows, for the proposed combination simulated and measured reflection and transmission data up to 3 GHz. Maximum/minimum transmission/return losses of 0.4 dB and 20 dB, respectively, have been achieved.

adding a resistor between the transistors. The new technique called a f_τ doubler, can overcome the previous problem and increase the bandwidth; however, the result is output power reduction and increased circuit complexity. In both papers [20], [21], shunt feedback technique has also been applied. It is well known that the shunt feedback technique increases bandwidth, stabilizes gain, and reduces distortion and influence of device tolerances. At the same time, input and output impedances can be controlled. We apply the shunt feedback technique to each individual single FET stage, together with multisection distributed matching networks using microstrip lines, as well as passive SMD devices to flatten and increase the bandwidth. Referring to Fig. 15, the feedback of each stage is defined by feedback resistances $R_{F1,2}$ and capacitances $C_{F1,2}$ where $C_{F1,2}$ are acting as pure dc blocks. The values of $R_{F1,2}$ that satisfy the required gain is given in [19] as

$$R_{F1,2} = Z_0 (1 + |S_{21}|_{1,2}) \quad \text{for } |R_{F1,2}| > Z_0 \qquad (4)$$

where $Z_0 = 50$ Ω and $|S_{21}|^2_{1,2}$ is the power gain of the stages. Unconditional stability $K > 1.3$ and improved broad-band performance can be obtained by adding a parallel combination of $R_{S1,2}$ and $C_{S1,2}$ in series at the input of each stage (see Fig. 15) where R_S is in the order of a few ohms.

The design of the matching network was started with the output network (OMN) synthesis as described in [22] and [23]. Initial load and source impedance values were taken from the load–pull analysis presented in Section III-A. Further goals of this first design cycle were little network complexity, gain flatness, an output return loss, and an output power of at least 10 dB and 5 W, respectively, over the full bandwidth. It has been found

that the design goal can be firstly achieved by a simple LC low-pass network. By this procedure, the load impedance of the ISMN (optimum source impedance of the SiC FET) was also found.

For the GaAs driver, FET load–pull analysis was also performed. The so-found load impedance, together with the source impedance of the SiC power FET, have been used as input data for synthesis and optimization of the ISMN with respect to maximum and flattened power transfer. A tapered microstrip line, together with a low-pass section, has been found as the most suitable solution.

The input matching network was found in a similar manner using a 50-Ω match and the GaAs FET input impedance as source and load impedances for the matching network. Three matching sections (a microstrip
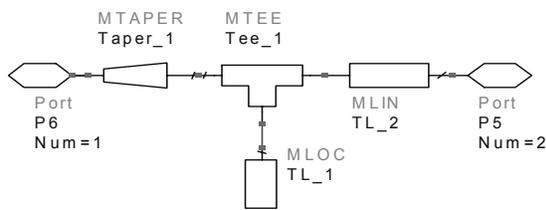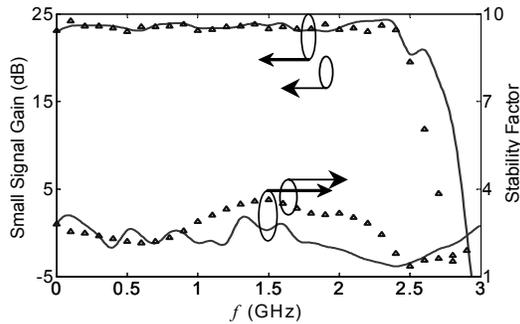

Fig. 16. Optimized ISMN topology based on ADS.

Fig. 17. Simulated and measured gain and stability factor.

line together with an open stub in low-pass form) had to be used at the input to realize the high-impedance transformation ratio necessary for matching the 50-Ω source impedance.

After finding the initial topologies and element values by the described procedures, the final design parameters were found by an overall optimization of all amplifier design parameters. During this final step, the described design strategy has been found to be very suitable. The circuit simulations were performed by using Agilent ADS. The substrate material data are based on ROGERS 4003 laminate with a permittivity of 3.38 and a thickness of 0.51 mm.

As an example of the designed matching networks, Fig. 16 illustrates the microstrip realization of the distributed ISMN. Similar input and output matching topologies are given in [13].

IV. EXPERIMENTAL RESULTS

The fabricated PA was characterized and the results were compared with simulations. Measurements, as long as not mentioned otherwise, were performed using a heat sink, which has kept the FET cases at room temperature. For the first time, a good agreement has been found. Small-signal S-parameters, power performances, two-tone measurements, AM–AM, AM–PM, and noise measurements are presented here.

A. Small Signal S-Parameters

Small-signal gain, stability factor, and input and output return losses were measured using a vector network analyzer. Bias data were $V_{D1} = 10$ V, $I_{D1} = 350$ mA, $V_{D2} = 40$ V, and $I_{D2} = 500$ mA, respectively. Fig. 17
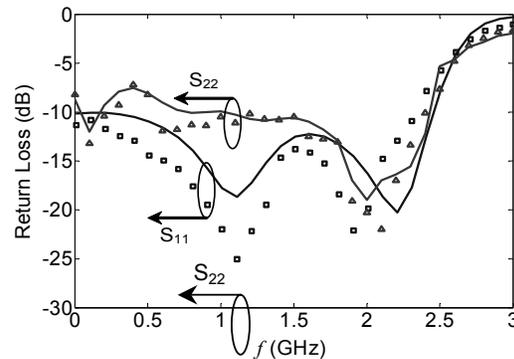

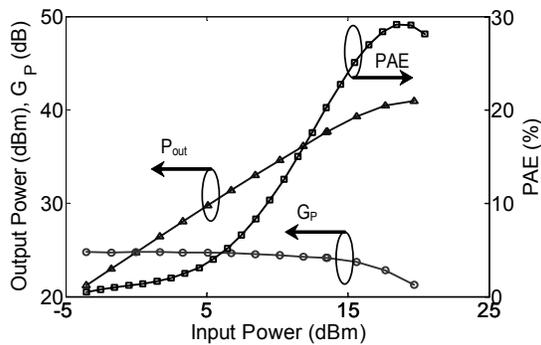Fig.18. Simulated (solid lines) and measured (symbols) return loss.
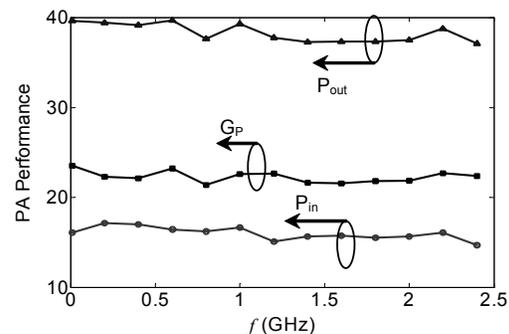

Fig. 19. Power performance measurements at 1 GHz.

Fig. 20. Power performance measurements versus frequency.

shows wide-band characteristics from 10 MHz to 2.4 GHz with a small-signal gain of 23 ± 1 dB and a stability factor $K > 1.3$. A very good agreement can be observed for the gain, whereas the measurement based K-factor is considerably higher. The reasons for that are additional losses of microstrip lines, surface mount devices (SMDs), and the substrate not precisely implemented enough in the related models.

Fig. 18 shows input and output return loss. Simulated and measured results match pretty well and the matching quality is satisfactory. The agreement between simulations and measurements could be improved by more precise modeling of SMD devices and discontinuities.

B. Power Performance

The power measurements were performed using an RF signal generator in conjunction with a medium PA as a power source. Fig. 19 shows output power, power gain, and PAE versus input power at 1 GHz for the bias
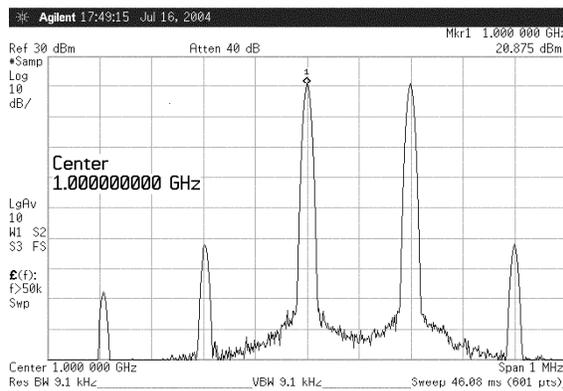

Fig. 21.   Two-tone measurement at $P_{in} = 0$ dBm, $f_0 = 1$ GHz, and $\Delta = 200$ kHz.
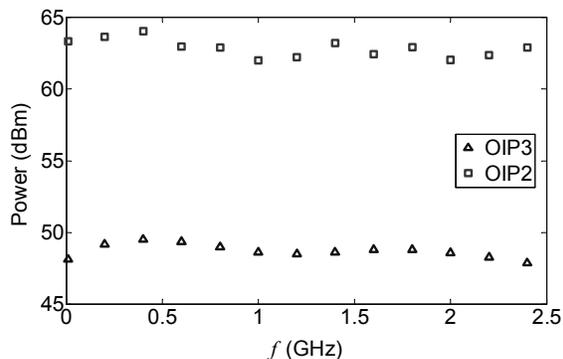

Fig. 22.   Measured linearity performance versus frequency.

parameters $V_{D1} = 10$ V, $I_{D1} = 350$ mA, $V_{D2} = 40$ V, and $I_{D2} = 500$ mA. From this figure, an output power of 37 dBm, power gain of up to 23 dB, and PAE of 28 % at 1 dB$_{CP}$ can be taken.

PA performance versus frequency is finally depicted in Fig. 20. Up to 2.4 GHz, an output power and power gain

of 37 dBm and 22 ± 1 dB (1 dB$_{CP}$), respectively, were obtained. The required input power at P$_{1dB}$ is also shown in Fig. 20.

C. Two-Tone Performance

The two-tone test was characterized by performing two-tone intercept point measurements. Two closely spaced input tones of equal amplitude were applied to the amplifier at f_0 and $f_0 + \Delta$, respectively, where Δ is the frequency spacing between the two tones.

The fundamental-, second-, and third-order components were determined using a spectrum analyzer as a function of input power.

An enhanced multitone signal generator (ESG, Agilent Technologies, Palo Alto, CA) was used to provide the two-tone signal at $f_0 = 1$ GHz with frequency spacing $\Delta = 200$ kHz and P$_{in} = 0$ dBm. The output amplitude spectrum was taken from the spectrum analyzer (PSA, Agilent Technologies), as shown in Fig. 21.
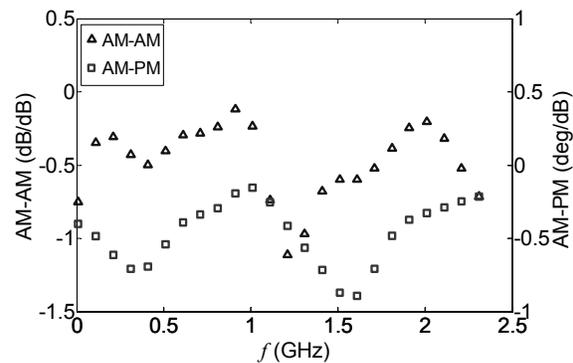
An input power sweep was applied and the output

Fig. 23.   Measured AM–AM (triangles) and AM–PM (squares) conversions of the two-stage PA versus frequency.

second-order intercept point (OIP2) and third-order intercept points (OIP3) were finally calculated using the equation

$$OIPn = \frac{P_{out} + \left(Harmonic\ Suppression\right)}{\left(n-1\right)} \quad (5)$$

where n is the order of the harmonic. The extracted second- and third-order intercept points at different frequencies are presented in Fig. 22. The diagram shows that minimum values of OIP2, and OIP3 of 61 and 48 dBm, respectively, have been achieved. Bias parameters were $V_{D1} = 10$ V, $I_{D1} = 350$ mA, $V_{D2} = 40$ V, and $I_{D2} = 500$ mA.

Fig. 22 shows that, compared to the SiC power stage alone (Fig. 9), the GaAs FET driver stage degrades the overall linearity performance. While the IP3 degradation was in the order of a couple of decibels, the IP2 performance degraded by approximately 10 dB. Although the overall linearity of the two-stage design is still very acceptable, we spend some effort to achieve a similar performance as for the power stage alone. We studied very careful the IP2 behavior of the GaAs FET

dependent on the operating point and source and load impedances. We have also improved the OIP2 performance from initially 50 dBm to over 60 dBm in the final design by few redesigns and proper settings of all parameters. However, all in all, we have to state that the chosen GaAs FET (Fujitsu FLL177ME) seems to not be the best choice for our application, especially not with respect to IP2 performance. We will spend further work for analysis of this issue taking into account other FET types and sizes.

D. AM–AM and AM–PM Distortions

Depending on the application, additional amplifier characterizations can give a more accurate representation of nonlinear distortions in an amplifier. Fig. 23 shows both amplitude and phase characteristics at 1 dB_{CP} versus frequency. The two-stage design exhibits AM–AM and AM–PM values of up to –1.2 (dB/dB) and –1 (deg/dB) over the full bandwidth. Both values are approximately twice the amount of the power stage alone and are, from that point-of-view acceptable. Although these values are also pretty low, they could be improved by a larger driver FET.

E. NF Measurements
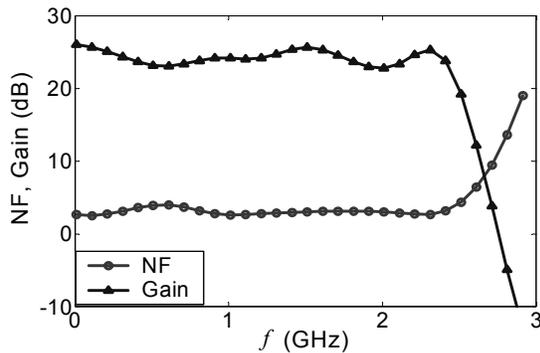
Although the NF does not belong to the important

Fig. 24.   Measured small-signal gain and NF versus frequency.

TABLE I
SUMMARY TWO-STAGE PA MEASUREMENTS

Parameter	Performance
Used Transistors	GaAs FET (Fujitsu) FLL177ME + SiC MESFET (Cree) CRF24010
Operating BW (GHz)	0.01…2.4
SS Gain (dB)	23 ± 1
Stability factor K	> 1.3
1 dB Output Power (dBm)	≥ 37
1 dB Power Gain (dB)	22 ± 1
PAE (%)	28
OIP2 (dBm)	≥ 61
OIP3 (dBm)	≥ 47
AM-AM (dB/dB)	≤ 1.2
AM-PM (deg/dB)	≤ 1
Noise Figure (dB)	≤ 4

parameters of a PA as the last function block in a transmitter chain, we nevertheless have characterized the noise properties. In Fig. 24, we show both small-signal gain and NF, which were measured using the Agilent spectrum analyzer (PSA) as an NF meter. Fig. 24 shows the results versus frequency. NF values below 4 dB over the whole bandwidth (typically 3 dB) have been achieved. This noise performance is excellent for a PA. The noise performance of the SiC power stage alone has also been measured, and it can be stated that it is worsen just by a few tenths of a decibel compared to the two-stage design. All performance data are summarized in Table I.

V. CONCLUSION

A two-stage 5-W wide-band RF PA has been designed using an SiC MESFET power stage covering the frequency range from 10 MHz to 2.4 GHz. A large-signal model has been developed and verified for the SiC device. Low-frequency dispersion and temperature behavior are included. 23 ± 1 dB small-signal gain has been achieved over the full bandwidth by combining feedback and matching circuits properly. Small-signal S-parameters, power performances, intermodulation characteristics, and NF data were measured, resulting in 22 ± 1 dB power gain, 37-dBm output power, 28 % PAE, > 47 dBm OIP3, and < 4 dB NF. Low sensitivity against AM–AM and AM–PM conversions has been noticed. Good agreement has been achieved between simulations and measurements. The SiC MESFET technology appears to be very suitable and reliable for power applications up to the lower gigahertz range.

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