APPLICATION NOTE

CGHV27015S, CGHV40100 Demonstration Power Amplifier, Operating from 50 to 1000 MHz.

Wolfspeed, a Cree Company, and Powerful Microwave Ltd. have developed an application circuit that demonstrates the wide bandwidth low frequency performance of the Cree CGHV40100F GaN HEMT. The circuit uses a CGHV27015S driving a CGHV40100F to obtain a power output of 100 watts over a frequency range of 50 MHz to 1,000 MHz. This application note describes the typical performance that has been achieved and which can be expected when evaluating the demonstrators. Details of the circuit are included for further understanding of the topology and all necessary information is provided to aid in reproduction of the amplifier. The reference circuit part numbers are 03-000325 = 50-1000 MHz, 15 W (driver); and 03-000326 = 50-1000 MHz, 100 W (PA). Key features of the resulting combined amplifier include:

- Wide Bandwidth covering 50 MHz - 1,000 MHz
- >18 dB Small Signal Gain from the Output Stage
- >30 dB Small Signal Gain from Driver and Output Stages
- >50 % Drain Efficiency
- 100 W Saturated Output Power
- Intended to be used with MilComm, TacCom applications

OVERALL DESIGN

The design goal for these application circuits was to provide a combined output power of 100 W, with 30 dB gain across 50 MHz to 1000 MHz. First, a test circuit has been designed to demonstrate the wideband performance of acts as a driver stage for the CGHV40100F. The driver amplifier demonstration circuit, designated as the 03-000325, is shown in Figure 1. The circuit is constructed using RO4350B circuit board material mounted on a 6mm aluminum plate. The bias sequencing circuit is also shown in Figure 1,
implemented on an FR4 PCB that is mounted perpendicular to the main RF circuit. The bias circuit provides the correct sequencing for the gate and drain voltages as well as over-temperature and over-current shutdown protection. The output stage power amplifier circuit board, part number 03-000326, is shown in Figure 2, along with its bias circuit.

![Output amplifier and bias control board.](image)

**Figure 2. Output amplifier and bias control board.**

**Driver Circuit**

The target for the driver stage was to achieve 100-1000 MHz bandwidth at an output power level of 10 W, suitable for driving the 100 W amplifier stage. In order to achieve flat gain over this range, shunt feedback was included in the design. To maximize bandwidth, very limited input matching has been incorporated in the test fixture. It is therefore recommended that an input attenuator be used to minimize interactions with the input signal source. In testing a 5 dB, 2 W SMA attenuator was used. Also, with the higher impedances at the lower power level, matching would require a transformer, which would introduce a frequency limitation. Figure 3 includes the schematic diagram of the driver circuit, along with a pictorial diagram of the board layout. The final design exceeds the performance objectives, delivering 15 W over 50-1000 MHz.

![Schematic diagram of the 03-000325 driver](image)

**Figure 3. Schematic diagram of the 03-000325 driver**
The bias to the device was adjusted from the pinched off gate to the voltage required for 60 mA Idq with no RF present; -2.71 V. The small signal performance of the 03-000325 with this bias, at 0 dBm input level, was measured and demonstrated a gain >18 dB from 1 to 1200 MHz (Figure 4).

![Driver Circuit Small Signal Performance - SN002](image)

Figure 4. Plot showing gain and other typical performance parameters for the driver circuit.

The unit is supplied with a bias sequencing and overcurrent protection board (Bias Board) which is mounted onto J3 of the test fixture and secured with two M2 screws. The operation of bias board is described in more detail below. The user may choose to operate the unit directly without the bias board. In this case, the gate bias voltage must be applied before the drain and re-moved after the drain voltage has fallen to 0 volts. This sequence prevents the power device from drawing excessive drain current. For additional protection, the drain supply current should be limited such that it cannot exceed 0.65 A at a drain voltage of 30 V. Note that the CGHV27015S can be operated at up to 50 V for saturated power operation but thermal limitations must be observed (see the device data sheet for more details).

**Bias and Protection Board**

This board provides a number of functions (see Figure 5):

A. Gate/Drain voltage sequencing  
B. Overcurrent protection  
C. Gate Voltage adjustment
D. Gate Voltage Temperature Compensation

E. Thermal shutdown/amplifier mute capability

F. Auxiliary +24 V, 150 mA supply (fan)

G. LED operation indicators for Gate, Drain, and Over-temperature.

As noted above, in order to prevent excess drain current it is important to establish the gate voltage before the drain voltage is applied to the transistor. On the bias and protection board a DC-DC converter produces a negative voltage from the +V supply. This is then passed through a linear voltage regulator which provides a stable negative voltage supply for the gate. The linear regulator also helps to minimize the switching spurs from the DC-DC converter, which is important because noise and other perturbations on the gate voltage will modulate the RF carrier and appear at the output of the amplifier. When the output of the linear regulator exceeds its defined limit, the drain control circuit is enabled as shown in Figure 6. At switch off, the reverse sequence is implemented; the drain voltage falls to 0 V before the gate shuts down, as seen in Figure 7.

Figure 5. Bias and Protection Board block diagram.

Figure 6. Drain on sequencing; there is a ~1.6 ms between the gate bias reaching its nominal voltage (blue trace) and the drain beginning to switch on (red trace).
B. OVER-CURRENT PROTECTION

Included in the Drain Voltage Control block is a current sense circuit. When the current exceeds 0.63 A (±5%) the overcurrent limit it will activate and switch off the drain supply. As a safety precaution, to reset the circuit the supply voltage must be removed for about 1 second. The current limit is determined by thermal dissipation of the transistor at 30 V drain voltage. Continuous operation at above this limit will cause overheating. It is possible that the user may wish to operate at a higher peak current, for example, using a pulsed or modulated RF where the average current will be below 0.63 A. In this case R8 on the bias board can be changed to a lower resistance. The current trip is initiated when the voltage drop across R8 exceeds 50 mV, thus the equation for R8 is:

\[ R8(\text{mΩ}) = \frac{50 \text{ mV}}{I \text{ (A)}} \]

R8 is a 2512 size precision 1 W current sense resistor.

Warning: changing R8 to a lower resistance risks damaging Q1 and additional average current limiting should be incorporated in the supply. Also, if operated from a 50 V supply the current limit needs to be decreased.

C. GATE VOLTAGE ADJUSTMENT

The gate voltage is nominally set to provide a quiescent drain current (Idq) of 50 mA, which gives the flattest overall gain response. This can be increased by the variable resistor, R18, on the bias board. Rotating clockwise makes the gate voltage less negative and increases the drain current. The nominal maximum gate voltage is -1.8 V which equates to a drain current of ~0.3 A. This may be done with a mechanical switch or by electronically pulling the pin to ground. The control sequence is shown in Figure 8; connections to the bias board are shown in Figure 9. It is strongly recommended that the user install a thermal switch or take other precautions to ensure that the amplifier is not operated at a temperature above 70°C.
D. Gate Voltage Temperature Compensation

The temperature compensation included on the bias circuit is intended to take into account long term temperature changes and is therefore located on the bias board. This is the other purpose (besides mechanical security) of the fixing screws for the bias board. Cree GaN typically exhibits a temperature response of 0.4 mV/°C. Experimentally, the temperature compensation has been optimized with R25 on the bias board of 5.1 kΩ, but this can be altered by the user if a different compensation slope is necessary. Increasing R25 reduces the temperature variation of the gate voltage. Note that if R25 is changed R18 may also require a slight adjustment for the required Idq.

E. Thermal Shutdown/Mute Capability

Space for a normally open thermal switch (Airpax 67F070) has been included on the assembly, but not supplied. This switch closes when the temperature exceeds 70°C. On the bias board there are two through holes within the area designated SW1 on the back of the bias board. If these are shorted together the bias board shuts down the drain supply, thus if the thermal switch SW1 pins are connected to these points (orientation does not matter) the driver amplifier will shut down if the switch temperature exceeds 70°C. When this occurs, the Red “OTEMP” LED will illuminate on the bias board.

These connections also may be used to Mute the amplifier without having to switch off the supply. This may be done with a mechanical switch or by electronically pulling the pin to ground. The control sequence is shown in Figure 8; connections to the bias board are shown in Figure 9. It is strongly recommended that the user install a thermal switch or take other precautions to ensure that the amplifier is not operated at a temperature above 70°C.

Figure 8. Thermal shutdown of drain supply line, note that the gate remains on during thermal shutdown.

Figure 9. Thermal switch or Mute connections to bias board. Both leads of the thermal switch must be connected to the two holes within the area outlined SW1 on the bias board.
F. Auxiliary (Fan) +24 V Supply

An additional 150 mA, +24 V supply primarily for a DC cooling fan has been included on the bias board (the connection is accessible from the pad marked “V1” on the driver board, on the left hand side of J3). Note that a ground return is also required. Loads that require more than 150 mA should not be used as this will cause excessive heating of U4 on the bias board.

G. LED Operation Indicators

The “Gate On” LED (orange) is illuminated when the negative supply rail exceeds ~ -2.5 V.

The “Drain On” LED (green) is illuminated when the drain is on and the supply rail exceeds +26 V. (Note that the drain LED may illuminate momentarily during the input voltage ramp but should be extinguished by the time the supply voltage reaches +5 V.)

The “OTemp” LED (red) is illuminated when either the thermal switch closes or the amplifier Mute is operated.

There is no specific indication when the overcurrent trip activates, however the “Drain On” will extinguish. To reset, the main supply line must be cycled off/on with a 1 second delay.

Output Stage Power Amplifier

To demonstrate the wideband performance of the CGHV40100F 100 W, 50 V, GaN HEMT, the demonstration circuit, labeled as the 03-000326 (Figure 10) was developed. Figure 11 shows the schematic with circuit elements defined for computer simulation. The target was to achieve 100-1000 MHz bandwidth at an output power level of 100 W. The circuit is constructed using RO4350B circuit board material mounted on a 6mm aluminum plate. The bias sequencing circuit is implemented on an FR4 PCB mounted

Figure 10. The 03-000326 100 W output stage and bias board.
perpendicular to the main RF circuit. As described above for the driver circuit, the bias circuit provides the correct sequencing for the gate and drain voltages as well as over-temperature and overcurrent shutdown protection.

The unit can deliver 100 W of CW power over the bandwidth by the appropriate selection of C12. As supplied, the unit is tuned for maximum bandwidth, with performance measurements shown in Figure 12. Increasing C12 to 8.6 pF will increase the power at 500 MHz to ≥100 W, but at the expense of power output above 900 MHz.

![Figure 11. Schematic diagram of the output stage.](image)

![Figure 12. Typical performance of the 03-000326 tuned for maximum bandwidth.](image)
In Figure 13, the blue trace shows the measured small signal (10 dBm drive level) gain and the purple trace the original simulated response. Taking the measurements of the input and output matching circuits and using these in the simulation produces the red trace, which we can see has the right shape but has ~1 dB higher loss across the band. The simulation was done with a gate bias voltage of -2.56 volts to get an Idq of 350 mA, however the simulation used -2.6 V for this current. If we set the gate to -2.6 V the current increases to 600 mA and we get a response as shown in the green trace, which is a very close match between measured and simulated.

![Figure 13. Small-signal gain—simulation and measurement results.](image)

Figure 14 includes plots of additional performance parameters, including current and drain efficiency over the bandwidth covered by the 03-000326 circuit, plus the saturated power output.

![Figure 14. Pin, Pout, current and Drain Efficiency of the 100 W application circuit](image)
Figure 16 shows the combined gain of the two stages with an input power of +15 dBm. The net gain plot includes the loss of the input attenuator.

![Figure 15. Saturated output power from the output stage at 50 V.](image)

![Figure 16. Gain of both stages combined with +15 dBm input, including the input attenuator.](image)

The unit is supplied with a bias sequencing and overcurrent protection board (Bias Board) which is mounted onto J3 of the test fixture and secured with two M2 screws. Although the operation of bias board is the same as described previously for the driver circuit, the operating parameters are different, as noted below. The user may choose to operate the unit without the bias board, but must take care that the alternate approach applies the gate bias voltage before the drain and removes it after the drain voltage has fallen to 0 volts. Also, the drain supply current should be limited such that it cannot exceed 5 A, (this is the limit imposed by the drain inductor, L4). The bias board is installed along the top of the 100 W amplifier board, plugged into connector J3.
The bias and sequencing board for the 100 W output stage amplifier provided, fulfils a number of functions similar to the bias and sequencing board mentioned for the driver stage:

A. Gate/Drain voltage sequencing  
B. Overcurrent protection  
C. Gate voltage adjustment  
D. Gate Voltage Temperature Compensation  
E. Thermal shutdown/amplifier mute capability  
F. Auxiliary (Fan) +24 V supply  
G. LED operation indicators for Gate, Drain, and Over-temperature.

A. GATE/DRAIN VOLTAGE SEQUENCING

In order to prevent excess drain current it is important to establish the gate voltage before the drain is applied to the transistor. On the bias and protection board a DC-DC converter produces a negative voltage from the +50 V supply. This is then passed through a linear voltage regulator which provides a stable negative voltage supply for the gate. When the output of the linear regulator exceeds a defined limit the drain control circuit is enabled. At switch off the reverse sequence is implemented; the drain voltage falls to 0 V before the gate shuts down.

B. OVERCURRENT PROTECTION

When the current exceeds 5 amps (±5%) the over-current limit will activate and switch off the drain supply. As a safety precaution, the supply voltage must be removed for about 1 second to reset the circuit. The current limit is determined by drain bias inductor L4; continuous operation at above 5 A will cause this inductor to overheat. It is possible that the user may wish to operate at a higher peak current, for example using a pulsed or modulated RF (where the average current will be below 5 A), in this case R8 on the bias board can be changed to a lower resistance. The current trip is caused by the voltage drop across R8 exceeding 50 mV, thus the equation for R8 is:

\[ R8(\text{mΩ}) = \frac{50 \text{ mV}}{I (A)} \]

R8 is a 2512 size precision, 1 W, current sense resistor.

Warning: changing R8 to a lower resistance, risks damaging the L4 and additional average current limiting should be incorporated in the supply.
C. Gate Voltage Adjustment

The gate voltage is nominally set to provide a quiescent drain current (Idq) of between 600 and 800 mA. This can be increased by the variable resistor, R18 on the bias board. Rotating clockwise makes the gate voltage less negative and increases the drain current. The nominal maximum gate voltage is ~-1.8 V which equates to a drain current of ~2.5 A.

D. Gate Voltage Temperature Compensation

The temperature compensation included on the bias circuit is intended to take into account long term temperature changes and is therefore located on the bias board. Cree GaN typically exhibit 0.4 mV/°C; experimentally the temperature compensation has been optimized with R25 on the bias board =5.1 kΩ, but this can be altered by the user if necessary. Increasing R25 reduces the temperature variation of the gate voltage. Note that if R25 is changed R18 may also require a slight adjustment for the required Idq.

E. Thermal Shutdown/Mute Capability

A normally open thermal switch has been included (but not wired in) on the 100 W amplifier assembly. This switch closes when the temperature exceeds 70°C. On the bias board there are two through holes within the area designated SW1 on the back of the bias board. If these are shorted together by the thermal switch the bias board shuts down the drain supply. When this occurs the Red “OTEMP” LED will illuminate on the bias board.

F. Auxiliary (Fan) +24 V Supply

As with the driver circuit's bias board, an additional 150 mA, +24 V supply primarily for a DC cooling fan has been included on the bias board, with the connection accessible from the pad marked “+V1” on the left hand side of J3. Note that a ground return is also required. Loads requiring more than 150 mA should not be used as this will cause excessive heating of U4 on the bias board.

G. LED Operation Indicators

The “Gate On”, “Drain On” and “OTemp” LEDs operate in the same manner as on driver circuit bias board. There is no specific indication when the overcurrent trip activates, however the “Drain On” will extinguish.

WANT MORE INFORMATION ABOUT THIS DESIGN?

To learn more about this design, watch this webinar at the Microwave Journal web site: “Practical Simulation and Design of Broadband GaN RF Power Amplifiers – How Close are We to Right First Time Now?”

http://www.microwavejournal.com/events/1250-practical-simulation-and-design-of-broadband-gan-rf-power-amplifiers-how-close-are-we-to-right-first-time-now
Driver Power Amplifier, 03-000325, Turn On Instructions

Using supplied bias board:

1. Connect bias board to J3 on 03-000325 and secure using two M2x6 screws and washers (provided). If thermal switch SW1 is to be used connect leads to bias board pins as described earlier (Figure 9).

2. Mount the amplifier test fixture, 03-000325, onto an adequate heatsink. At 10 W RF output and 50% drain efficiency the unit will dissipate 10 W of heat, note that the heatsink should be sufficient to keep the base plate to <50°C under normal operation. Four 4mm diameter holes are included in the fixture for mounting on the heat sink.

3. Ensure that the output of the 03-00325 is connected to a suitable 50Ω load via an appropriately rated cable. If being used to drive the 03-00326, J2 may be connected directly to the input SMA connector of the 03-00326. If mounted on the same heatsink the connectors should be at the same height.

4. With the input (J1) terminated in 50Ω connect the Red wire to the +50 V (positive) terminal of the power supply and the Black wire to the supply ground (negative) terminal. The power supply should be rated at >0.6 A minimum current rating. Gradually increase the supply voltage to 30 V and observe the current drawn. This should be ~50 mA with no RF, rotating R18 counter-clockwise will make the gate voltage more negative and reduce the quiescent current Idq.

5. Switch off the supply and connect the RF input (J1) to a low level input signal of ~0 dBm (5-1200 MHz) and observe the gain shape, which should be similar to Figure 18.

Figure 17. Typical small-signal (0 dBm) performance of the driver circuit at 30 V and Idq of 50 mA.
6. Increase the drive level and verify the performance with the test results provided, see Figure 12 for typical performance. Note that the unit may require a suitably power rated attenuator if the low input return loss causes issues with the signal source. In testing a 5 dB 2 W attenuator was used.

7. To achieve higher power levels mid-band (at the expense of top end performance) the open circuit stub on the input (opposite R1) can be shortened.

**Using directly connected power supplies:**

Note that the correct sequencing of the applied voltages is essential to avoid damaging the transistor. Care must be taken during switch on and off to ensure that the gate voltage is established before applying the drain voltage and is maintained until the drain voltage is removed.

The connections for the supply to J3 are as follows:

- Vdrain (pins 3 & 8)
- Vgate (pin 1)
- Ground (pins 2, 4, 7 & 9)

The red and black supply wires can be used for the drain if pins 5 & 6 are joined to 3 & 8. The current capability of the drain and ground wires must be 0.8A each (minimum).

I. With all of the power supplies switched off connect the positive terminal of the gate supply to the negative terminal of the drain supply and the ground return from 03-000325. Connect the gate to the negative terminal of the gate supply. Connect the drain to the positive terminal of the drain supply.

II. Terminate the RF input (J1) and output (J2) in suitably rated 50Ω loads and mount the unit on a suitable heatsink as described in (2) above.

III. Adjust the gate supply to -5 V. Turn on the gate bias power supply.

IV. Starting at 0 V turn on the drain power supply and gradually increase the voltage to +30 V. No current should be drawn from the supply.

V. Adjust the gate supply gradually until the quiescent drain current (Idq) reaches 50 mA; typically the current will not start to increase until the gate voltage reaches -3.0 V.

VI. Continue as with (5), (6), & (7) of the bias board operating procedures.

VII. When switching off, remove the RF input signal, decrease the drain voltage to 0 V and switch off the drain supply before switching off the gate supply.
Using supplied bias board:

1. Connect bias board to J3 on 03-000326 and secure using two M2x6 screws and washers (provided). If thermal switch SW1 is to be used connect leads to bias board pins as described earlier.

2. Mount the amplifier test fixture, 03-000326, onto an adequate heatsink. At 100 W RF output and 50% drain efficiency the unit will dissipate 100 W of heat, note that the heatsink should be sufficient to keep the base plate to <50°C under normal operation. Eight 4 mm diameter holes are included in the 03-000326 for mounting on the heat sink. For optimal heat transfer a thin layer of heat sink compound or a Pyrolytic Graphite Sheet (PGS) thickness <0.1 mm, can be used between the base plate of 03-000326 and the heatsink.

3. Ensure that the output of the 03-000326 is connected to a suitable 50Ω load via an appropriately rated cable. Excessive mechanical stress on the output connector J2 should be avoided.

4. With the input (J1) terminated in 50Ω connect the Red wire to the +50 V (positive) terminal of the power supply and the Black wire to the supply ground (negative) terminal. The power supply should be rated at 5 A minimum current rating. Gradually increase the supply voltage to 50 V and observe the current drawn. This should be <800 mA with no RF, rotating R18 counter-clockwise will make the gate voltage more negative and reduce the quiescent current Idq.

5. Switch off the supply and connect the RF input (J1) to a low level input signal of ~10 dBm (5-1200 MHz) and observe the gain shape, which should be similar to Figure 18.

![Figure 18. Typical small-signal performance of the 100 W circuit at 50 V.](image)
6. Increase the drive level and verify the performance with the test results provided, see Figure 12 for typical performance.

7. To achieve higher power levels mid-band (at the expense of bandwidth) increase the effective value of C12 by adding additional capacitance. Typically adding ~4.7 pF (ATC800B recommended) will produce 100 W at 500 MHz. Note that the capacitors are usually mounted on their sides to avoid parasitic resonances.

**Using directly connected power supplies:**

Note that the correct sequencing of the applied voltages is essential to avoid damaging the transistor. Care must be taken during switch on and off to ensure that the gate voltage is established before applying the drain voltage and is maintained until the drain voltage is removed.

The connections for the supply to J3 are as follows:

- Vdrain (pins 3 & 8)
- Vgate (pin 1)
- Ground (pins 2, 4, 7 & 9)

The red and black supply wires can be used for the drain if pins 5 & 6 are joined to 3 & 8. The current capability of the drain and ground wires must be 6A each (minimum).

I. With all of the power supplies switched off connect the positive terminal of the gate supply to the negative terminal of the drain supply and the ground return. Connect the gate to the negative terminal of the gate supply. Connect the drain to the positive terminal of the drain supply.

II. Terminate the RF input (J1) and output (J2) in suitably rated 50Ω loads and mount the unit on a suitable heatsink as described in (2) above.

III. Adjust the gate supply to -5 V. Turn on the gate bias power supply.

IV. Starting at 0V turn on the drain power supply and gradually increase the voltage to +50 V. No current should be drawn from the supply.

V. Adjust the gate supply gradually until the quiescent drain current (Idq) reaches 600 mA; typically the current will not start to increase until the gate voltage reaches -3.0 V.

VI. Continue as with (5), (6), & (7) of the bias board operating procedures.

VII. When switching off, remove the RF input signal, decrease the drain voltage to 0V and switch off the drain supply before switching off the gate supply.
<table>
<thead>
<tr>
<th>Ident</th>
<th>Value</th>
<th>Qty</th>
<th>Part Number</th>
<th>Manufacturer</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C5</td>
<td>470 pF</td>
<td>2</td>
<td>ATCB00B471KT200X</td>
<td>ATC</td>
<td>200V Hi Q</td>
</tr>
<tr>
<td>C4</td>
<td>2400 pF</td>
<td>1</td>
<td>C08BL242X-5ZN-X0B</td>
<td>DiLabs</td>
<td>50V Broadband</td>
</tr>
<tr>
<td>C2, C6</td>
<td>1000 pF</td>
<td>2</td>
<td>MC0805B102K101CT</td>
<td>FEC 1759287</td>
<td>100V, X7R 0805 Ceramic Cap</td>
</tr>
<tr>
<td>C3, C7</td>
<td>10 nF</td>
<td>2</td>
<td>C0805C103K1RACTU</td>
<td>FEC 1844409</td>
<td>100V, X7R 0805 Ceramic Cap</td>
</tr>
<tr>
<td>R1</td>
<td>270 R</td>
<td>1</td>
<td>CRCW0603270RFKEA</td>
<td>FEC 2141320</td>
<td>Chip Resistor, 0603 0.1W, 1%</td>
</tr>
<tr>
<td>R2, R3</td>
<td>390 R</td>
<td>2</td>
<td>CRGH2512J390R</td>
<td>FEC 2331928</td>
<td>Chip Resistor, 2512 2W, 5%</td>
</tr>
<tr>
<td>F1</td>
<td>470 R</td>
<td>1</td>
<td>BLM18PG471SN1D</td>
<td>Murata</td>
<td>Ferrite Bead, 0603 1A</td>
</tr>
<tr>
<td>L1</td>
<td>100 nH</td>
<td>1</td>
<td>1008HQ-R10XJLB</td>
<td>Coilcraft</td>
<td>Rf Inductor, 5%</td>
</tr>
<tr>
<td>L2</td>
<td>3.5 uH</td>
<td>1</td>
<td>4310LC_352KEB</td>
<td>Coilcraft</td>
<td>RF High Current Inductor</td>
</tr>
<tr>
<td>Q1</td>
<td>15 W</td>
<td>1</td>
<td>CGHV27015S</td>
<td>Cree</td>
<td>50 V 15 W GaN HEMT</td>
</tr>
<tr>
<td>J1, J2</td>
<td>SMA(F)</td>
<td>2</td>
<td>142-0701-881</td>
<td>Emerson</td>
<td>SMA edge launch</td>
</tr>
<tr>
<td>J3</td>
<td>10 Way</td>
<td>1</td>
<td>9578-101-10LF</td>
<td>RS 6737332</td>
<td>10W 2R 2.54mm 3A</td>
</tr>
<tr>
<td>J4</td>
<td>2 Way</td>
<td>1</td>
<td>1-2106003</td>
<td>RS 7184837</td>
<td>IDC 2W 20AWG</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PFRM_PCB_TF0013</td>
<td>PFRM</td>
<td>PCB RO4350B</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PFRM_BP_TF0013</td>
<td>PFRM</td>
<td>Base Plate</td>
</tr>
<tr>
<td>M2 x 6</td>
<td></td>
<td>1</td>
<td>M26 CSSTMCZ100</td>
<td>FEC 1419409</td>
<td>Screw, Slit, Cheese, Steel</td>
</tr>
<tr>
<td>M2</td>
<td></td>
<td>1</td>
<td>D00822</td>
<td>FEC1613999</td>
<td>Crinkle Washer S/S</td>
</tr>
<tr>
<td>M2</td>
<td></td>
<td>1</td>
<td>Brass Flat Washer</td>
<td>FEC 1377534</td>
<td>Brass Flat Washer</td>
</tr>
<tr>
<td>M2.5 x 6</td>
<td></td>
<td>10</td>
<td>M2.56 CSSTMCZ100</td>
<td>FEC1419411</td>
<td>Screw, Slit, Cheese, Steel</td>
</tr>
<tr>
<td>M2.5</td>
<td></td>
<td>10</td>
<td>D01132</td>
<td>FEC1624023</td>
<td>Spr. Washer, S/Coil Br. Zinc</td>
</tr>
<tr>
<td>M2.5</td>
<td></td>
<td>10</td>
<td>Brass Flat Washer</td>
<td>FEC 1377535</td>
<td>Brass Flat Washer</td>
</tr>
<tr>
<td>M3 x 12</td>
<td></td>
<td>A/R</td>
<td>M312 PSSTMCZ100</td>
<td>FEC1419293</td>
<td>Screw, Slit, Cheese, Steel</td>
</tr>
<tr>
<td>M3</td>
<td>A/R</td>
<td>1</td>
<td>D01133</td>
<td>FEC1624024</td>
<td>Spr. Washer, S/Coil Br. Zinc</td>
</tr>
<tr>
<td>M3</td>
<td>A/R</td>
<td></td>
<td>Brass Flat Washer</td>
<td>FEC 1377536</td>
<td>Brass Flat Washer</td>
</tr>
</tbody>
</table>

Data Sheet for the CGHV27015S GaN HEMT
http://www.wolfspeed.com/cghv27015s
<table>
<thead>
<tr>
<th>Ident</th>
<th>Value</th>
<th>Qty</th>
<th>Part Number</th>
<th>Manufacturer</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>12 pF</td>
<td>1</td>
<td>600S120GT250X</td>
<td>ATC</td>
<td>250V Hi Q RF Ceram Cap</td>
</tr>
<tr>
<td>C2</td>
<td>2400 pF</td>
<td>1</td>
<td>C08BL242X-5ZN-X0B</td>
<td>DiLabs</td>
<td>50V Broadband</td>
</tr>
<tr>
<td>C3</td>
<td>3.9 pF</td>
<td>1</td>
<td>600S3R9BT250X</td>
<td>ATC</td>
<td>250V Hi Q RF Ceram Cap</td>
</tr>
<tr>
<td>C4</td>
<td>20 pF</td>
<td>1</td>
<td>600S200JT250X</td>
<td>ATC</td>
<td>250V Hi Q RF Ceram Cap</td>
</tr>
<tr>
<td>C5, 10</td>
<td>6.8 pF</td>
<td>2</td>
<td>600S6R8BT250X</td>
<td>ATC</td>
<td>250V Hi Q RF Ceram Cap</td>
</tr>
<tr>
<td>C9</td>
<td>390 pF</td>
<td>1</td>
<td>800B391KT200X</td>
<td>ATC</td>
<td>200V Hi Q RF Ceram Cap</td>
</tr>
<tr>
<td>C7, 11</td>
<td>100 pF</td>
<td>2</td>
<td>MC0805B102K101CT</td>
<td>FEC1759287</td>
<td>100V, X7R 0805 Ceramic Cap</td>
</tr>
<tr>
<td>C6, 8</td>
<td>10 nF</td>
<td>2</td>
<td>C0805C103K1RACTU</td>
<td>FEC1844409</td>
<td>100V, X7R 0805 Ceramic Cap</td>
</tr>
<tr>
<td>C12</td>
<td>SOT</td>
<td>1</td>
<td>800B (3.9 pF nom.)</td>
<td>ATC</td>
<td>200V Hi Q RF Ceram Cap</td>
</tr>
<tr>
<td>R1-4</td>
<td>110 R</td>
<td>4</td>
<td>3521110RFT</td>
<td>FEC2117478</td>
<td>Chip Resistor, 2512 2W, 1%</td>
</tr>
<tr>
<td>R5, 6</td>
<td>18 R</td>
<td>2</td>
<td>CRCW120618R0FKEA</td>
<td>FEC2139271</td>
<td>Chip Resistor, 1206 .25W, 1%</td>
</tr>
<tr>
<td>R7</td>
<td>10 R</td>
<td>1</td>
<td>RC0603-FR-0710RL</td>
<td>FEC9238247</td>
<td>Chip Resistor, 0603 .1W, 1%</td>
</tr>
<tr>
<td>FT1</td>
<td>12-50Q</td>
<td>1</td>
<td>XTM0310B5012</td>
<td>Anaren</td>
<td>Ferrite Transformer</td>
</tr>
<tr>
<td>L1-3</td>
<td>82 uH</td>
<td>3</td>
<td>1515SQ-82N</td>
<td>Coilcraft</td>
<td>RF Inductor, 5%</td>
</tr>
<tr>
<td>L4</td>
<td>1.3</td>
<td>1</td>
<td>4310LC_132KEB</td>
<td>Coilcraft</td>
<td>RF High Current Inductor</td>
</tr>
<tr>
<td>Q1</td>
<td>100W</td>
<td>1</td>
<td>CGHV40100F</td>
<td>Cree</td>
<td>50V 15 GaN HEMT</td>
</tr>
<tr>
<td>CL1</td>
<td></td>
<td>1</td>
<td>4-001578-4</td>
<td>Cree</td>
<td>Transistor Cap</td>
</tr>
<tr>
<td>J1</td>
<td>SMA(F)</td>
<td>1</td>
<td>142-0701-881</td>
<td>Emerson</td>
<td>SMA edge launch</td>
</tr>
<tr>
<td>J2</td>
<td>N (F)</td>
<td>1</td>
<td>R161410520</td>
<td>Radiall</td>
<td>N 0.5” Flange</td>
</tr>
<tr>
<td>J3</td>
<td>10 Way</td>
<td>1</td>
<td>95278-101-10LF</td>
<td>FCI</td>
<td>10W 2R 2.54mm 3A/pin</td>
</tr>
<tr>
<td>J4</td>
<td>2 Way</td>
<td>1</td>
<td>1-2106003</td>
<td>TE Connectivity</td>
<td>IDC 2W 20AWG</td>
</tr>
<tr>
<td>SW1</td>
<td>N/O</td>
<td>1</td>
<td>67F070</td>
<td>Airpax</td>
<td>Norm Open 70°C Thermostat</td>
</tr>
</tbody>
</table>

Data Sheet for the CGHV40100 GaN HEMT
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