CAB760M12HM3
1200 V, 760 A All-Silicon Carbide
High Performance, Switching Optimized, Half-Bridge Module

Technical Features

- Low Inductance, Low Profile 62mm Footprint
- High Junction Temperature (175 °C) Operation
- Implements Switching Optimized Third Generation SiC MOSFET Technology
- Light Weight AlSiC Baseplate
- High Reliability Silicon Nitride Insulator

Applications

- Railway & Traction
- Solar
- EV Chargers
- Industrial Automation & Testing

System Benefits

- Lightweight, Compact Form Factor with 62mm Compatible Baseplate Enables System Retrofit
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- High Reliability Material Selection

Key Parameters \( (T_c = 25 ^\circ C \text{ unless otherwise specified}) \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Conditions</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{DS \text{ max}} )</td>
<td>Drain-Source Voltage</td>
<td>1200</td>
<td>A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{GS \text{ max}} )</td>
<td>Gate-Source Voltage, Maximum Value</td>
<td>-8</td>
<td>+19</td>
<td></td>
<td>V</td>
<td>Transient, &lt;100 ns</td>
<td>Fig. 32</td>
</tr>
<tr>
<td>( V_{GS \text{ op}} )</td>
<td>Gate-Source Voltage, Recommended Op. Value</td>
<td>-4</td>
<td>+15</td>
<td></td>
<td></td>
<td>Static</td>
<td></td>
</tr>
<tr>
<td>( I_D )</td>
<td>DC Continuous Drain Current</td>
<td>1015</td>
<td></td>
<td></td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_S )</td>
<td>DC Source-Drain Current</td>
<td>765</td>
<td></td>
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<tr>
<td>( I_{SD \text{ (pulsed)}} )</td>
<td>DC Source-Drain Current (Body Diode)</td>
<td>515</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{DS \text{ (pulsed)}} )</td>
<td>Maximum Pulsed Drain-Source Current</td>
<td>1530</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{SD \text{ (pulsed)}} )</td>
<td>Maximum Pulsed Source-Drain Current</td>
<td>1530</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>( T_{VJ \text{ op}} )</td>
<td>Maximum Virtual Junction Temperature under Switching Conditions</td>
<td>-40</td>
<td>175</td>
<td></td>
<td>°C</td>
<td></td>
<td></td>
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</tbody>
</table>

Note 1 Assumes \( R_{JH,JC} = 0.068^\circ C/W \) and \( R_{DS(on)} = 2.13 \text{ m}\Omega \). Calculate \( P_o = (T_{VJ} - T_c) / R_{JH,JC} \). Calculate \( I_{D_{\text{MAX}}} = \sqrt{(P_o / R_{DS(on)})} \).
### MOSFET Characteristics (Per Position) \( (T_{\text{J}} = 25 ^\circ \text{C unless otherwise specified}) \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Conditions</th>
<th>Note</th>
</tr>
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<tbody>
<tr>
<td>( V_{\text{BRDSS}} )</td>
<td>Drain-Source Breakdown Voltage</td>
<td>1200</td>
<td>1.8</td>
<td>2.5</td>
<td>3.6</td>
<td>( V )</td>
<td></td>
</tr>
<tr>
<td>( V_{\text{GS(th)}} )</td>
<td>Gate Threshold Voltage</td>
<td></td>
<td>0.12</td>
<td>2.0</td>
<td>3.6</td>
<td>( V )</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{DSS}} )</td>
<td>Zero Gate Voltage Drain Current</td>
<td></td>
<td>15</td>
<td>400</td>
<td>( \mu A )</td>
<td>( V_G = 0 \text{ V, } V_{\text{DS}} = 1200 \text{ V} )</td>
<td></td>
</tr>
<tr>
<td>( I_{\text{GS}} )</td>
<td>Gate-Source Leakage Current</td>
<td></td>
<td>0.12</td>
<td>3</td>
<td>( \mu A )</td>
<td>( V_G = 15 \text{ V, } V_{\text{DS}} = 0 \text{ V} )</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{DS(on)}} )</td>
<td>Drain-Source On-State Resistance (Devices Only)</td>
<td></td>
<td>1.33</td>
<td>1.73</td>
<td>( \text{m} \Omega )</td>
<td>( V_G = 15 \text{ V, } I_D = 760 \text{ A} )</td>
<td>Fig. 2, Fig. 3</td>
</tr>
<tr>
<td>( g_{\text{m}} )</td>
<td>Transconductance</td>
<td></td>
<td>548</td>
<td>585</td>
<td>( S )</td>
<td>( V_G = 20 \text{ V, } I_{\text{DSS}} = 760 \text{ A} )</td>
<td>Fig. 4</td>
</tr>
<tr>
<td>( E_{\text{On}} )</td>
<td>Turn-On Switching Energy, ( T_J = 25 ^\circ \text{C} )</td>
<td></td>
<td>20.3</td>
<td>20.7</td>
<td>23.7</td>
<td>( \text{m} )</td>
<td>( V_G = 600 \text{ V, } V_{\text{DS}} = 4 \text{ V/15 \text{ V, } R_{\text{G}(\text{ext})} = 1.0 \Omega, } L = 13.6 \mu \text{H} )</td>
</tr>
<tr>
<td>( E_{\text{Off}} )</td>
<td>Turn-Off Switching Energy, ( T_J = 25 ^\circ \text{C} )</td>
<td></td>
<td>17.9</td>
<td>17.5</td>
<td>17.8</td>
<td>( \text{m} )</td>
<td>( V_G = 800 \text{ V, } V_{\text{GS}} = -4 \text{ V/15 \text{ V, } I_G = 760 \text{ A} )</td>
</tr>
<tr>
<td>( R_{\text{G(int)}} )</td>
<td>Internal Gate Resistance</td>
<td>0.47</td>
<td>0.47</td>
<td>0.47</td>
<td>( \Omega )</td>
<td>( T_J = 25 ^\circ \text{C} )</td>
<td></td>
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<tr>
<td>( C_{\text{iss}} )</td>
<td>Input Capacitance</td>
<td>79.4</td>
<td>79.4</td>
<td>79.4</td>
<td>( \text{nF} )</td>
<td>( V_{\text{GS}} = 0 \text{ V, } V_{\text{DS}} = 800 \text{ V, } V_{\text{AC}} = 25 \text{ mV, } f = 100 \text{ kHz} )</td>
<td>Fig. 9</td>
</tr>
<tr>
<td>( C_{\text{oss}} )</td>
<td>Output Capacitance</td>
<td>2.9</td>
<td>2.9</td>
<td>2.9</td>
<td>( \text{pF} )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{\text{rss}} )</td>
<td>Reverse Transfer Capacitance</td>
<td>90</td>
<td>90</td>
<td>90</td>
<td>( \text{pF} )</td>
<td></td>
<td></td>
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<tr>
<td>( Q_{\text{GS}} )</td>
<td>Gate to Source Charge</td>
<td>768</td>
<td>768</td>
<td>768</td>
<td>( \text{nC} )</td>
<td>( V_{\text{DS}} = 800 \text{ V, } V_{\text{GS}} = -4 \text{ V/15 \text{ V, } I_G = 760 \text{ A} )</td>
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<tr>
<td>( Q_{\text{GD}} )</td>
<td>Gate to Drain Charge</td>
<td>924</td>
<td>924</td>
<td>924</td>
<td>( \text{nC} )</td>
<td></td>
<td></td>
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<tr>
<td>( Q_{\text{G}} )</td>
<td>Total Gate Charge</td>
<td>2724</td>
<td>2724</td>
<td>2724</td>
<td>\text{pF}</td>
<td></td>
<td></td>
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<tr>
<td>( R_{\text{th,JC}} )</td>
<td>FET Thermal Resistance, Junction to Case</td>
<td>0.068</td>
<td>0.073</td>
<td>0.073</td>
<td>( ^\circ \text{C/W} )</td>
<td></td>
<td>Fig. 17</td>
</tr>
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### Module Physical Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Test Conditions</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{1-2}$</td>
<td>Package Resistance, M1</td>
<td>106.5</td>
<td></td>
<td></td>
<td>μΩ</td>
<td>$T_c = 125^\circ C$, Note 2</td>
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<tr>
<td>$R_{2-3}$</td>
<td>Package Resistance, M2</td>
<td>126.3</td>
<td></td>
<td></td>
<td>μΩ</td>
<td>$T_c = 125^\circ C$, Note 2</td>
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<tr>
<td>$L_{stray}$</td>
<td>Stray Inductance</td>
<td>4.9</td>
<td></td>
<td></td>
<td>nH</td>
<td>Between Terminals 1 and 3</td>
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<tr>
<td>$T_c$</td>
<td>Case Temperature</td>
<td>125</td>
<td></td>
<td></td>
<td>°C</td>
<td></td>
<td></td>
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<tr>
<td>$W$</td>
<td>Weight</td>
<td>179</td>
<td></td>
<td></td>
<td>g</td>
<td></td>
<td></td>
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<tr>
<td>$M_s$</td>
<td>Mounting Torque</td>
<td>3</td>
<td>4.5</td>
<td>5</td>
<td>N-m</td>
<td>Baseplate, M6 bolts</td>
<td>Note 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.9</td>
<td>1.1</td>
<td>1.3</td>
<td></td>
<td>Power Terminals, M4 bolts</td>
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<tr>
<td>$V_{isol}$</td>
<td>Case Isolation Voltage</td>
<td>4</td>
<td></td>
<td></td>
<td>kV</td>
<td>AC, 50 Hz, 1 min</td>
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<tr>
<td>CTI</td>
<td>Comparative Tracking Index</td>
<td>600</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Clearance Distance</td>
<td>13.07</td>
<td></td>
<td></td>
<td>mm</td>
<td>Terminal to Terminal</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Terminal to Baseplate</td>
<td>6.00</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Terminal to Terminal</td>
<td>14.27</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Terminal to Baseplate</td>
<td>12.34</td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Note 2 Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(ON)} +$ Switch Position Package Resistance.
Typical Performance

Figure 1. Output Characteristics for Various Junction Temperatures

Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

Figure 3. Normalized On-State Resistance vs. Junction Temperature

Figure 4. Transfer Characteristic for Various Junction Temperatures

Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 15$ V

Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 0$ V (Body Diode)
Typical Performance

Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = -4$ V (Body Diode)

Figure 8. Typical Capacitances vs. Drain to Source Voltage ($0$ - $200$ V)

Figure 9. Typical Capacitances vs. Drain to Source Voltage ($0$ - $1200$ V)

Figure 10. Threshold Voltage vs. Junction Temperature

Figure 11. Switching Energy vs. Drain Current ($V_{DS} = 600$ V)

Figure 12. Switching Energy vs. Drain Current ($V_{DS} = 800$ V)
Typical Performance

Figure 13. MOSFET Switching Energy vs. Junction Temperature

Figure 14. Reverse Recovery Energy vs. Junction Temperature

Figure 15. MOSFET Switching Energy vs. External Gate Resistance

Figure 16. Reserve Recovery Energy vs. External Gate Resistance

Figure 17. MOSFET Junction to Case Transient Thermal Impedance, $Z_{tjc}$ (°C/W)

Figure 18. Forward Bias Safe Operating Area (FBSOA)
Typical Performance

Figure 19. Reverse Bias Safe Operating Area (RBSOA)

Figure 20. Continuous Drain Current Derating vs. Case Temperature

Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)
Figure 23. Timing vs. Source Current

Figure 24. Timing vs. External Gate Resistance

Figure 25. Timing vs. Junction Temperature

Figure 26. dv/dt and di/dt vs. Source Current

Figure 27. dv/dt and di/dt vs. External Gate Resistance

Figure 28. dv/dt and di/dt vs. Junction Temperature
Definitions

Figure 29. Turn-off Transient Definitions

Figure 30. Turn-on Transient Definitions

Figure 31. Reverse Recovery Definitions

Figure 32. $V_{GS}$ Transient Definitions
Schematic and Pin Out

Package Dimension (mm)

<table>
<thead>
<tr>
<th>PIN</th>
<th>LABEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V4</td>
</tr>
<tr>
<td>2</td>
<td>Fwd</td>
</tr>
<tr>
<td>3</td>
<td>V</td>
</tr>
<tr>
<td>4</td>
<td>G1, Top row pins (2)</td>
</tr>
<tr>
<td>5</td>
<td>K1, Bottom row pins (2)</td>
</tr>
<tr>
<td>6</td>
<td>G2, Top row pins (2)</td>
</tr>
<tr>
<td>7</td>
<td>K2, Bottom row pins (2)</td>
</tr>
<tr>
<td>8</td>
<td>NTC1</td>
</tr>
<tr>
<td>9</td>
<td>NTC2</td>
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</table>
Supporting Links & Tools

- CGD1700HB3P-HM3 Evaluation Gate Driver
- CGD12HB00D: Differential Transceiver Board
- CPWR-AN-35: Thermal Interface Material Application Note
- KIT-CRD-CIL12N-HM: Dynamic Performance Evaluation Board for the HM2 and HM3 Module

Notes

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, or air traffic control systems.

- The SiC MOSFET module switches at speeds beyond what is customarily associated with IGBT-based modules. Therefore, special precautions are required to realize optimal performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford optimal switching time and avoid the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and DC link capacitors to avoid excessive VDS overshoot.